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Modeling and control of emerging DC-DC topologies for renewable energy applications

A dissertation presented by

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Dedication

To my lovely family, who has always been there for me.

My parents Rosa and Javier.

My sister Alexandrina and her husband Joaquin.

To Leonardo and Valentina.

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Modeling and control of emerging DC-DC topologies for renewable energy applications

by

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Abstract

Renewable energy is attracting investigation and investment worldwide. This can be notice by studying cases of countries such as, Germany, China or Sweden , which are making big investment in this field, brief information about these and other European countries that are in the top ten of the renewable energy generation are presented.

The main topic in this dissertation is the penetration of renewable energy into the grid, since it has been increasing considerably over the years. In this topic, it is involve the study of DC-DC and DC-AC power conversion. In this dissertation the DC-DC power conversion stage is studied in detail. Conventional DC-DC topologies are used in the industry in this DC-DC power conversion stage, however, these topologies have some limitations. For that reason, new topologies have been emerging, their characteristics represent an improvement over the limitations of conventional DC-DC topologies. Considering that, in this dissertation some of the emerging topologies, their modeling and control are studied. Moreover, it will be discuss how the interconnection of the renewable energy source is usually made, and how a stepping-up converter is incorporated into the system, and what are the main characteristics of this converter in order to have proper exploitation of the source. Also, it is considered that renewable energy sources are intermittent sources, which is undesirable since it may imply interruptions to the electrical supply, to overcome this issue, a set of controllers are proposed. Finally, not only the theoretical aspects are discussed, but also the hardware implications. A brief explanation of the chapters included in this dissertation is presented next:

In Chapter 2 a novel control technique ”Minimum Current-Ripple Point Tracking” is presented, which is an output current/voltage control for interleaved DC-DC converters with dual switched input-inductors, i.e., interleaved input inductors controlled by independent switches. The controller for the interleaved converter encompasses three control stages: current stabilization, output-voltage regulation and minimum input-current-ripple control. In contrast with the two first loops, the latter is a novel stage introduced in this work to allow operation with minimum input-current-ripple in the whole operating region. That is, even though the converter has been designed for operation with minimum ripple in a given operating point, the scheme is able to dynamically deviate from this point to a new one where the ripple is minimized and the output voltage remains constant.

In Chapter 3 it is shown how this new MCRPT control strategy is applicable to the study of double dual boost converters, in which discrete-time linear and non-linear controllers are presented. Under the proposed linear control technique, a new stability condition and gain

tuning methodology are presented. Moreover, a nonlinear discrete-time controller is proposed in case of requiring performance optimization over a wider signal range.

In Chapter 4, the MCRPT control strategy is tested in a Proton-Exchange Membrane Fuel Cell (PEMFC) . A discrete-time controller is selected for this purpose. In this way, the converter can mitigate the harmonic distortion on the current extracted from the PEMFC, which is beneficial to improve the efficiency and lifetime of the cell.

In Chapter 5 the MCRPT control technique is combine with a nonlinear controller.

In Chapter 6 a strategy to regulate the charge and discharge of ultracapacitors in electric vehicles applications is explained.

In Chapter 7 a controller that is able to stabilize DC-DC converters feeding a constant load is studied.

Chapter 8 explains in detail the modeling of a DC-DC, this converter has the necessary characteristics for renewable energy. Finally, in Chapter 9 the conclusions of this dissertation are presented. The proposed controllers for the DC-DC converters are validated with experimental results, in which scale prototypes were designed.

Contents

Chapter 1

Introduction

High-power converters started with gate-turn-off (GTO) thyristors with the commercial development of 4500 volts switching devices. These GTO devices became the standard until the development of the high-power insulated-gate bipolar transistors (IGBTs) and gate-commutated thyristors (GCTs) in the 1990s. These switching devices have improved switching characteristics, like reduced power losses, ease of gate control, and snubberless operation, which make them optimal for high-power applications [1]. Out of the development in the high-power switches, power electronics is an area in constant development, nowadays it is involved in many applications, such as automotive, illumination, battery backup systems, renewable energy sources and many others.

In this dissertation, the DC-DC converter, which is a power electronics component, are studied, and how it improves the penetration of renewable energy into the grid. These DC-DC converters are a part of the hybrid inverter, the latest is usually incorporated to have a proper interconnection between the renewable energy source and the grid. A lot of topologies of DC-DC converters are available in the literature, depending on the application, each topology has advantages over the others. Considering that the application of the hybrid inverter previously mentioned is for renewable energy, their main characteristics needs to be considered.
Firstly, it is common that renewable energy is generated at low voltages, which makes it inconvenient to have a direct connection with the grid. Then a DC-DC topology with the ability to increase the input voltage is required. For this reason, some DC-DC converters have been proposed to step-up voltages in an efficient and reliable way [4–6]. Among the desirable features of such converters are the use of moderate duty cycles to maintain high-efficiency.
Added to this, this step-up stage has an inherent characteristic associated, which is the input current ripple [2,3]. This ripple is undesirable, since it represents a low efficiency and a decay in the lifetime of some sources. Renewable DC sources such as fuel cells and solar panels are between the sources that produce low output voltages and are affected by this input current ripple.
Secondly, renewable energy such as solar or wind has a fluctuating output voltage, due to their own nature, for this, the converter must be incorporated with a control stage. The principal objective of this controller is to maintain a constant output voltage under disturbances of the system, either if it is a input voltage (as a consequence of renewable energy variations) or a load variation (as a consequence of the demand that the system may have). In this dissertation

the control design considers that a fixed operation point is required, but also a system with a wide operating range is studied.
Common solutions for these inconvenient features of renewable energy are commercially available, nevertheless, the use of conventional topologies is highly extended. The inconvenient with these conventional topologies is that they deliver a restricted output voltage, that is, they have limited gain. Moreover, the input current ripple cancellation is also limitated to a specific point, which is a disadvantage considering that renewable energy sources are not constant. For these reasons, in this dissertation, instead of conventional topologies, emerging topologies for renewable energy applications are considered. These emerging topologies have some advantages over the conventional, like a higher gain and a better ripple cancellations characteristics. The use of these emerging topologies imply some challenges, like their modeling and control. For this, in this dissertation, a proper modeling technique and a adequate control strategy are proposed.

1.1 Motivation

Since 2000, the production of renewable energy has been increasing over the years worldwide, as can be appreciated in Fig. 1.1, these data was obtained from [7]. In this graph it can be appreciated how the wind and solar energy production are becoming relevant. Nevertheless, hydropower is by far the most common renewable energy source.

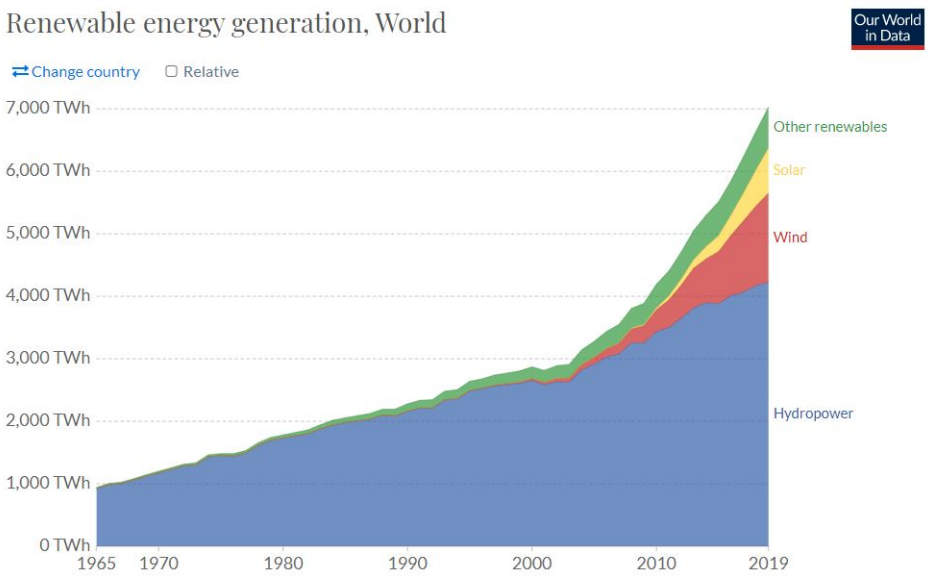

Figure 1.1: Renewable energy generation worldwide.

To have a better understanding on the distribution of this renewable energy production, Fig. 1.2 is shown, in this figure a world map where each country is colored according to the amount of renewable energy production is shown. It can be appreciated how the blue countries are between the most contributors to this matter. Most of the blue colored countries are due to

the hydraulic reserves they have. But other countries colored in green, such as some European countries, are increasing their solar and wind energy production, i.e. Germany or Sweden.

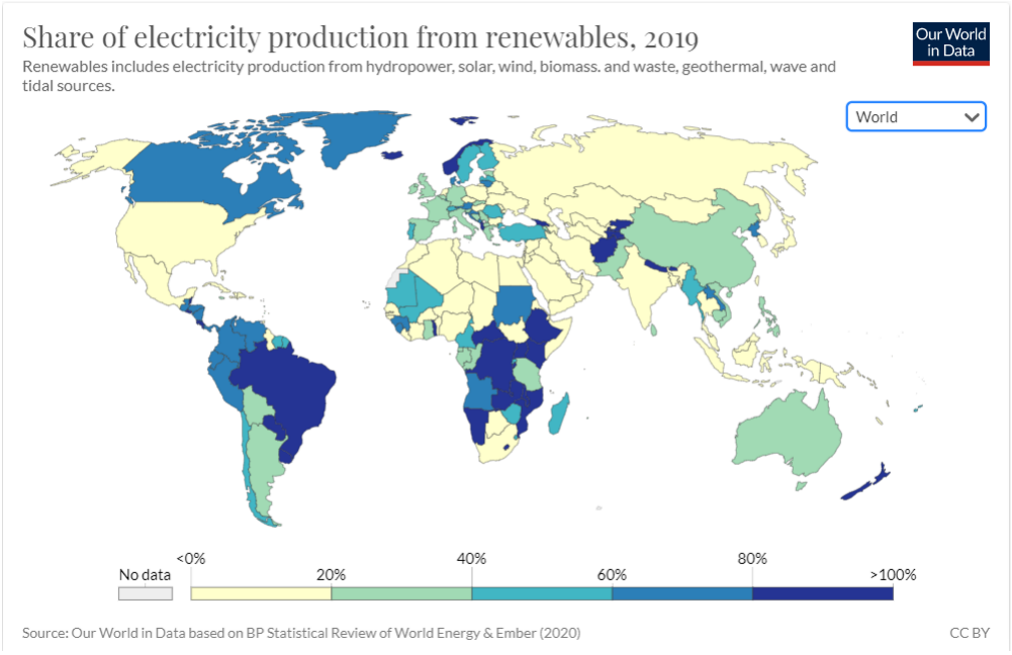

Figure 1.2: Share of electricity production from renewable energy worldwide.

A constant increase in the global consumption of energy must be a concern for all countries all over the world. Some countries have a better progress in this matter like it was appreciated in Fig. 1.2. This environmental compromise is recorded by the Energy Trilemma Index, a document that the World Energy Council updates every year. In 2016 the three first places were: Denmark, Switzerland and Sweden, respectively, while Mexico was in the 52 place [8]. In the year of realization of this dissertation (2020), the top ten of the rank is still dominated by OECD countries, whit the top three as follows: Switzerland, Sweden, Denmark, while Mexico is in the 45 place. The top ten of this ranking is dominated by European countries, this top ten rank illustrates the benefit of longstanding active energy policies [8].

It can be appreciated how the European countries become the leaders in renewable energies, particularly from wind generation. From this top three, it can be appreciated the case of Denmark, which is a great example of how the fossil fuels can be replaced by renewable energy sources. Denmark is a leader in generation of power from wind, it is far away from his nearest rival, which is Ireland, the latest have 28% of its power from wind generation, while Denmark recorded a 47% of power generated by wind [9]. It is surprising how these European countries from the top of renewable energy generation accomplished their goals, that is the case of Sweden, which is a country in constant growing with the objective of 100% of renewable energy production by the year of 2040, which may be seem so ambitious, but considering that in 2012, Sweden reached the government´s objective of 50% [10], it seems to be plausible.

But renewable energy can also be obtained from the sun. A remarkable example on solar energy is Germany, which is also in the top ten of the Energy Trilemma Index, as can be

appreciated in the Fig. 1.3, which was obtained from [11], most of the installed capacity are solar and wind energy.

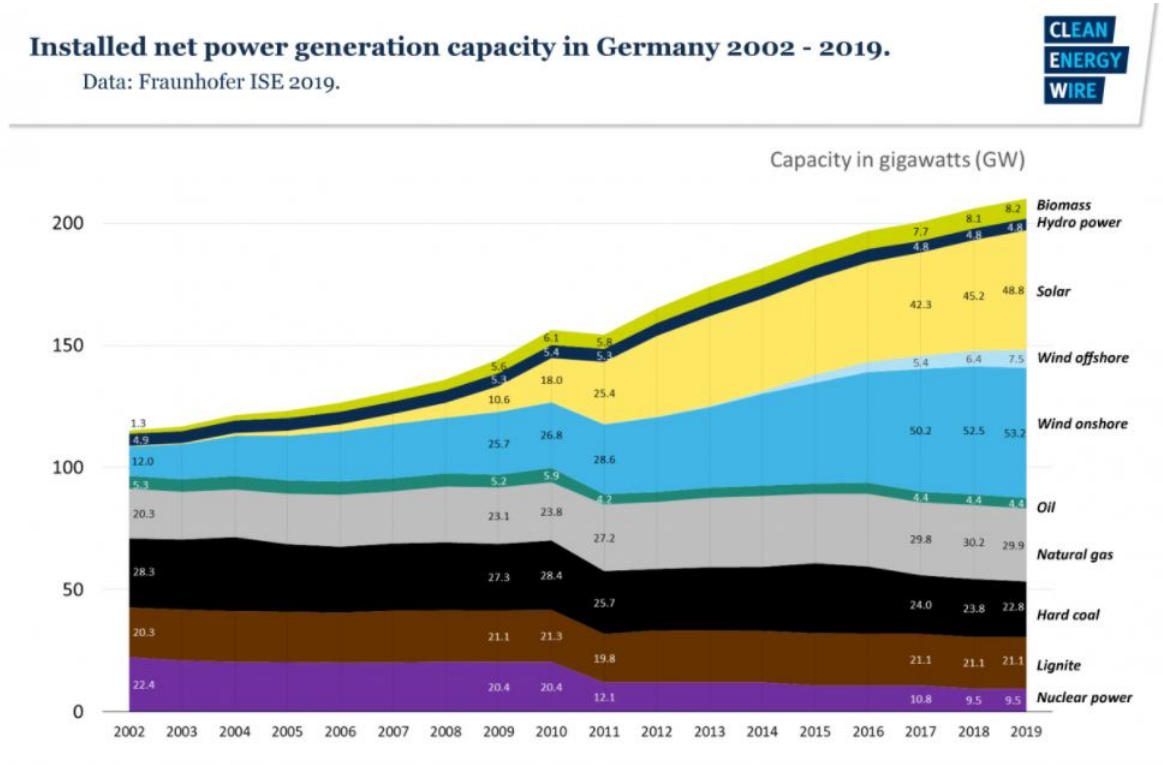

Figure 1.3: Installed net power generation capacity in Germany 2002-2019.

It is possible to continue remarking the best countries in renewable energy exploitation, but it is clear that clean energy is the global tendency around the world. Or eventually will be for some countries that are not still compromise with the environment.

1.2 Problem Statement and Context

We have seen how the energy industry is making big changes due to new technologies and new environmental concerns, this implies new challenges to the electrical industry. The incorporation of these new technologies into the existing electrical system is the main objective of recent studies.

While studying renewable energy sources incorporation to the grid, the power transfer is one of the main objects of study. This is, how to improve the efficiency of the system to exploit the maximum power from the source. As was previously discussed, renewable energy sources have some inherent characteristics that limits their exploitation; one of these is the low voltage that these sources produces, to solve this issue, extra components need to be included in the system, the most common solution for this, is the use of power transformers. Nevertheless, in the area of power electronics, analogous devices to power transformers are

object of study, namely the power converters. One of the main advantages over the classical power transformers, is the possibility to convert direct current to direct current (DC-DC). A variety of power converters are available, this variation is a result of how the components are connected to form each topology. Since our primary objective is to increase the voltage of the source, topologies with this ability are desired. The basic step-up converter is the well-known boost converter, shown in Fig. 1.4. Nevertheless, as shown in Fig. 1.5 [2] the output voltage of this boost converter, which can be refereed as a conventional topology, is limited. As the output voltage of the converter increases (i.e. the duty cycle of the converter reaches value of 1) the gain (V_{out}/V_g) tends to zero. Then, a proper topology, with the basic principle of stepping-up the voltage as the boost topology does, but with a higher gain at the same duty cycle, in order to avoid extreme duty cycles, needs to be selected to overcome the low voltage of the renewable energy source.

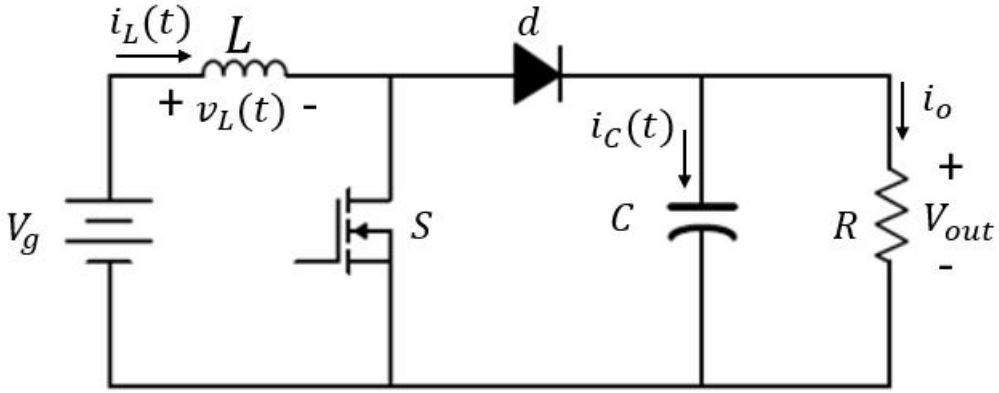

Figure 1.4: Boost converter.

In addition to the low output voltage of conventional topologies, the input current ripple of these topologies tends to be unacceptable to have a proper utilization of the energy available from the power source. A typical waveform of this ripple is shown in Fig. 1.6 [2]. In this figure the input current ripple expected from a conventional boost topology is assigned as Δi_L. As previously said, this ripple is undesirable because it represents the wasted energy from the source, also it affects the efficiency and lifetime of some renewable energy sources, such as solar panels or fuel cells. This decrees in efficiency of solar panels was recorded in [12], the result can be appreciated in Table 1.1, where an open loop experiment was carried out and Table 1.2, where the results of a closed loop are shown. The input current ripple cancellation is a common topic in the literature, some of this literature use the conventional topology in combination with extra components, like passive filters or coupled inductors. In this dissertation non conventional topologies are selected to overcome this input current ripple cancellation.

The use of new topologies imply new challenges, like their modeling. The modeling of conventional topologies is well documented. Averaging is a recurrent modeling technique

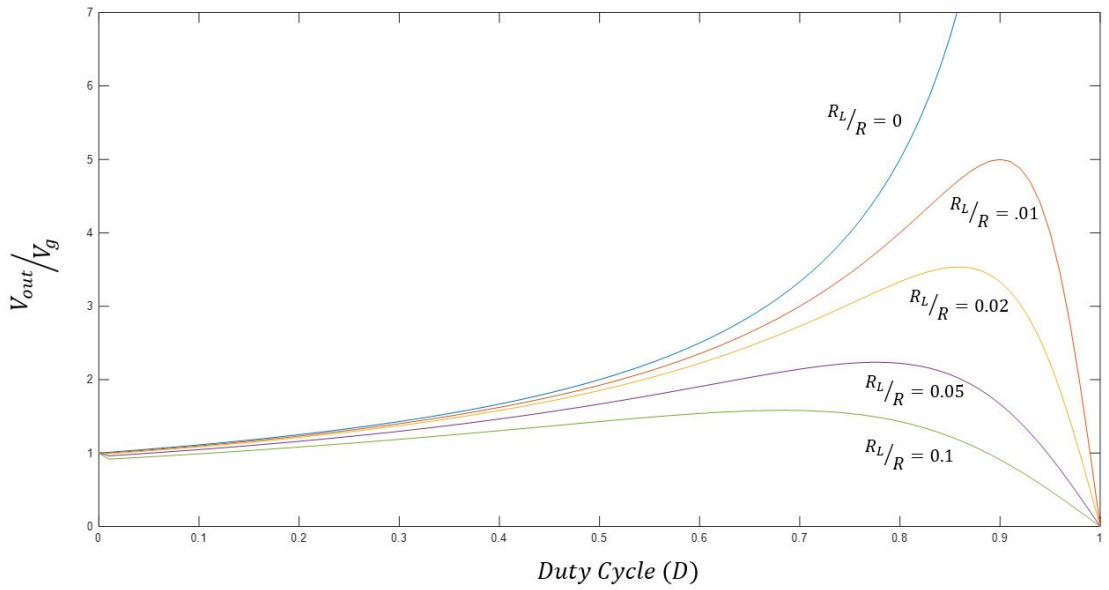

Figure 1.5: Output voltage vs duty cycle in a boost converter.

with a lot of advantages to avoid dealing with differential equations. Nevertheless, this technique is not applicable in some cases, for example when capacitors are in parallel connection. These parallel capacitors are essential in DC-DC converters with multiplier stages. Then new modeling techniques need to be performed.

As was previously discussed, the DC-DC converter must have a proper control to deal with intermittences to the system, while maintaining constant output voltage. Since some of the step-up converters are a result of the main principle of the conventional boost topology, they share a non-minimum phase characteristic with respect to the output voltage, that is, the transfer function has a zero in the right half plane. This characteristic limits their control bandwidth, to deal with this non-minimum phase, a proper controller needs to be selected.

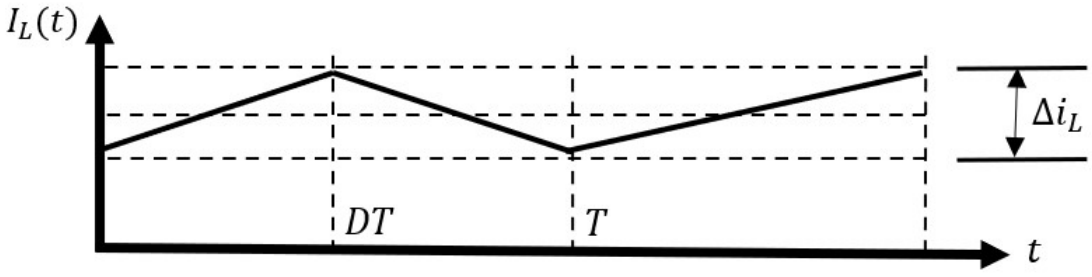

Figure 1.6: Input-current ripple of a boost converter.

In this dissertation these drawbacks of renewable energy sources are solved, first by

Open loop		
% Isc	P_{avg}	% eff
5	133.3	98
10	127.7	93.9
20	118.1	86.8
30	109.5	80.5
40	102.8	75.6
50	97.6	71.8
60	92.8	68.3
70	89.1	65.4
80	81.9	60.2
90	77.6	57.1

Table 1.1: Relation between input ripple current and the solar panel efficiency.

Closed loop		
% Isc	P_{avg}	% eff
5	132.3	97.3
10	129.9	95.5
20	127.6	93.8
30	122.2	89.8
40	116.2	85.5
50	110.3	81.1
60	103.3	76.0
70	96.7	71.1
80	74.7	54.9
90	41.4	30.4

Table 1.2: Relation between input ripple current and the solar panel efficiency.

selecting a topology that is capable of producing a greater output voltage than conventional topologies, and second, the input current ripple is minimized, in this way the lifetime and efficiency of the renewable energy source are improve. Added to these improvements, in this dissertation, the control of the power converter is designed in such way that even when some of the renewable energy sources are intermittent, the power transfer is able to be in a continuous form.

1.3 Objectives

The objectives of this work can be summarized as follows:

- Develop modeling techniques applicable to emerging DC-DC topologies.
- Study and develop control strategies considering the necessities of renewable energy.
- Develop new control tuning techniques applicable to the topologies used in this dissertation.
- Propose and develop a ripple cancellation technique according to the topologies used in this dissertation.
- Develop the ability to test and corroborate theoretical results via hardware implementation.
- Prove that the proposed techniques are useful in real renewable energy applications.

1.4 Solution overview

The main challenges of renewable energy sources and their implications on the DC-DC topology were discussed in previous sections. The necessity for high gain, the input current ripple

cancellation, new modeling strategies, and a proper control are the primary objectives of this dissertation.

Instead of using the conventional boost topology, along this document, two emerging topologies with the desired ccharacteristics for a proper exploitation of renewable energy, will be discuss; firstly, a topology named *"Interleaved Multilevel Boost Converter"*, and secondly, a topology named *"Double Dual Boost Converter"*; these two topologies selected, have in common a high gain property, and a input current ripple cancellation capability. For the modeling of these topologies, along this dissertation a continuous mode of operation is considered, that is, the current of the converter is greater than zero all the time. An important contribution for the modeling of these emerging topologies, is that they were analyzed in such way, that even when the number of components in the converter increases with respect to conventional topologies, the resultant model is quite similar in complexity. The control for these topologies was designed considering the non-minimum phase characteristics previously discussed, then a minimum-phase variable was selected to implement the control, that is, the input current of the converters, nevertheless, since the variable to be controlled is the output voltage, then an external control loop is added to the first current control loop, in that way, the converter is stable and the output voltage remains constant.

Since all of the proposed techniques of this dissertation needs to be implemented, the discrete-time modeling of these topologies is studied. In this dissertation, an approximate discrete-time model is proposed, in which a nonlinear set of equations are employed. This modeling allows the use of a nonlinear controller, that is also exposed.

Along this document, some publications are presented. Each of these publications deals with a specific issue previously described.

- In Chapter 2, the *"Interleaved Multilevel Boost Converter"* is presented, its modeling strategy is discussed, and the topology is combined with a new control strategy, that ensures an active minimization in the input current ripple.
- In Chapter 3, a linear and a nonlinear discrete-time controllers are presented. In this article an approximate discretization process is presented. Also, a new stabilizing condition is discussed as a new tuning control technique. These two contributions are demonstrated on a *"Double Dual Boost Converter"*, which is an emerging topology with a ripple cancellation capability, reason why an implicit current ripple cancellation technique is considered.
- In Chapter 4, the input current ripple cancellation control strategy presented in Chapter 1 is tested under the operation of a fuel cell, moreover, the control strategy is performed in discrete-time. The main objective of this article, is to proved how the technique improves the extraction of energy from a fuel cell. That is, the proposed techniques are applicable to real renewable energy sources.
- In Chapter 5 the ripple technique presented in Chapter 1, is combined with a nonlinear controller, proving that it is possible to combine this technique with another type of controllers.

- In Chapter 6 a strategy to manage the energy available in electric vehicles is presented. Due to the penetration of hybrid electric vehicle in the electrical system, it is an important topic to deal with.
- In Chapter 7, the study of DC-DC converters feeding constant power loads is presented.
- In Chapter 8, the modeling of the *"Interleaved Multilevel Boost Converter"* is discussed in detail and the control,of this topology, which is a topology with proper characteristics for interconnection of renewable energy sources, is presented.

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Chapter 2

Minimum Current-Ripple Point Tracking Control for Interleaved Dual Switched-Inductor DC-DC Converters

Summary of the chapter

In this chapter a research journal that presents a novel output current/ voltage control for interleaved DC-DC converters with dual switched input-inductors, i.e., interleaved input inductors controlled by independent switches is presented. The proposed approach is able to guarantee a minimum input-currentripple point tracking (MCRPT) despite of variations on the operating point. The controller encompasses three control stages: current stabilization, output-voltage regulation and minimum input-current-ripple control. In contrast with the two first loops, the latter is a novel stage introduced in this work to allow operation with minimum input-current-ripple in the whole operating region. That is, even though the converter has been designed for operation with minimum ripple in a given operating point, the scheme is able to dynamically deviate from this point to a new one where the ripple is minimized and the output voltage remains constant. The proposed scheme is experimentally validated using a laboratory prototype of a high-gain interleaved multilevel boost converter.

Minimum Current Ripple Point Tracking Control for Interleaved Dual Switched-Inductor DC–DC Converters

Carlos A. Villarreal-Hernandez, Omar Fernando Ruiz-Martinez, Jonathan Carlos Mayo-Maldonado, Gerardo Escobar, *Senior Member, IEEE*, Jesus Elias Valdez-Resendiz, and Julio C. Rosas-Caro

***Abstract*—This article presents a novel output current/voltage control for interleaved dc–dc converters with dual switched input inductors, i.e., interleaved input inductors controlled by independent switches. The proposed approach is able to guarantee a minimum input current ripple point tracking despite of variations on the operating point. The controller encompasses three control stages: current stabilization, output-voltage regulation, and minimum input current ripple control. In contrast with the two first loops, the latter is a novel stage introduced in this article to allow operation with minimum input current ripple in the whole operating region. That is, even though the converter has been designed for operation with minimum ripple in a given operating point, the scheme is able to dynamically deviate from this point to a new one where the ripple is minimized and the output voltage remains constant. The proposed scheme is experimentally validated using a laboratory prototype of a high-gain interleaved multilevel boost converter.**

***Index Terms*—Control, current ripple, interleaved dc–dc converters, modeling.**

I. Introduction

RENEWABLE dc sources such as fuel cells, solar panels, etc., usually produce low and fluctuating output voltages, that are not suitable to directly feed grid-tied inverters. Consequently, dc–dc converters with high input-to-output voltage gain are required [1]–[3]. Among the desirable features of such converters, the use of moderate duty cycles to maintain high-efficiency is required, which is not possible to achieve with traditional converters. Another relevant issue in renewable energy applications is the converter's input current ripple [4], which is an inherent component in boost converters playing a major role in efficiency and life-time of, e.g., photovoltaic (PV) panels and fuel cells (cf. [5], [6]).

It is precisely this issue that has motivated the flourishing of ripple-cancellation strategies where interleaved topologies (see e.g. [7]–[16]) are the most appealed solutions. However, it has been noticed that high input-to-output voltage gain solutions and input current ripple cancellation topologies are topics commonly studied separately (with a few existing plausible rounded approaches, e.g., [17]). In addition, a common shortcoming in interleaved converters is the restriction of having a fixed operating point at which the current-ripple is perfectly cancelled. This restriction implies that the duty cycle, and consequently the converter gain, cannot be freely selected, usually $D = 0.5$. Hence, the current-ripple is reduced but not cancelled out outside a relatively small neighborhood of the zero current-ripple operating point. The following are examples of this restriction.

In [7]–[9], the authors propose controllers based on current-balancing and output voltage regulation with a restricted operating point. In [17], a linear controller for a double-dual boost converter is implemented, where duty cycles of the transistor stages are required to be equal. The work in [18] presents a linear controller that achieves perfect cancellation at a constrained operating point, with equal inductor currents. In [19], a linear closed-loop implementation that requires equal duty cycles is presented. In [20], a controller that involves proportional values duty cycles is presented. Needless to say, the closed-loop operation of the converters is crucial to deal with variations of, both input-voltage and load that are present in any realistic scenario (see e.g., [7], [18]–[21]).

In some cases, the aforementioned constraint is enforced by interleaved topologies, where, although their input inductors are controlled by different switches, such switches cannot adopt arbitrary duty cycles. This is the case of, for example, the traditional two phase interleaved boost converter. However, there are other modern topologies that contain dual input inductors, where inductors are independently controlled, as in *double dual boost converters* (see [17], [22]). This is also the case in many other topologies, see e.g., the review of interleaved converters in [23]. Motivated by this issue, the pivotal argument in this article, is that there is no compelling reason to keep constraining

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the duty cycles in modern interleaved converters. Instead, this article proposes to exploit their emerging freedom coming from duality, to increase the current ripple cancellation capabilities of converters over a much wider operating region.

From the literature review, it has been observed that high input-to-output voltage gain converters, input current ripple mitigation and the appropriate control design are relevant topics for which there is still room for improvement. This article presents a complete solution for the above discussed issues, which comprises an interleaved topology of two multilevel dc–dc boost converters together with an appropriate controller overcoming disadvantages of some high input-to-output voltage gain topologies, and featuring input current ripple mitigation at any desirable operating region. It is shown that all these are achieved by the proper sizing of inductors and a suitable control law that minimizes the input current ripple in an *active* way.

In particular, a new control strategy is proposed, which is able to simultaneously regulate the output voltage and actively mitigate the input current ripple despite of variations in the operating point. Out of this, a new concept referred to as *minimum current ripple point tracking (MCRPT)* for interleaved converters is introduced. That is, the proposed control scheme steers duty cycles to a particular steady-state value, where the minimum possible input current ripple is guaranteed with respect to any operating point of a voltage-regulated converter. In order to do so, we provide the characterization of converter gains that ensure stability in terms of easy-to-construct LMIs, for which effective computational tools to find solutions can be used, such as the MATLAB toolbox `Yalmip`. The proposed scheme and the main theoretical achievements are validated via experimental results.

II. Main Contributions

The contributions of the proposed MCRPT controller can be outlined as follows.

1) *Active minimization of the current ripple is achieved*. Which permits to operate the converter over a region instead of only an operating point, which is the traditional point of view in passive strategies.
2) *The proposed control is dual*. i.e., it permits to independently set up the controllers, which drops the restriction to use a single time constant. This permits a greater disturbance rejection capability since one controller is able to respond faster than the other, out of which the lagging effect of the dominant (slowest) time constant is bypassed.
3) *Stability is rigorously guaranteed*. This is supported via the above Lyapunov analysis and the fact that the proposed converter has only one equilibrium point (characterized by the gain equations), i.e., given a single equilibrium, local stability implies global stability.
4) *There is room for accommodating further current/voltage regulation strategies*. i.e., it is possible to replace current/voltage loops by other strategies or to select the gains in a different way. This can be done if additional objectives or optimization strategies are of special interest for a particular application.

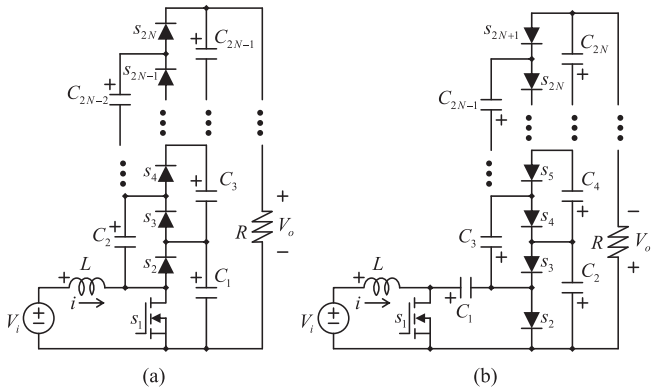

Fig. 1. (a) Multilevel boost converter. (b) Three-switch high voltage multilevel converter.

5) *Further performance specifications can be easily accommodated*. The proposed controller gain computation in terms of *linear matrix inequalities* (LMIs), permits to add further restrictions in the sense of optimal control. For instance, the LMI representation of functionals to enforce energy, time response, voltage/current variable relationships, and so forth.

III. Interleaved Multilevel Boost Converter

This section deals with the introduction and the modeling of a nonconventional *switched-capacitor* topology, where standard modeling techniques, such as *averaging* (in the sense of [24]), cannot be directly applied. This is a known shortcoming that is extensively discussed in [25]–[27]. To deal with this issue, we resort to a special nonstandard *averaging* technique based on a *reduced-order modeling* approach (see [27]–[29] with other plausible variations) that is instrumental for control purposes. The proposed interleaved topology is based on the combination of the multilevel boost converter proposed in [30] [see Fig. 1(a)] and a multilevel circuit derived from the Cuk converter proposed in [31] [see Fig. 1(b)]. These are hybrid topologies as they both comprise a step-up converter and multilevel stages based on switched capacitor multiplier cells. The resulting converters feature high gain, small size, high power density, and light weight due to the low voltage stress across (small size) components.

A. Interleaved Multilevel Boost Converter

By interleaving the configurations in Fig. 1, the topology shown in Fig. 2 is obtained, which is referred to as the *interleaved multilevel boost converter* all along the article. The modeling of these type of topologies involves several challenges. First, an increased number of stages implying an increased number of equations; and second, a switched-capacitor dynamics, which cannot be modeled right away by *averaging* (cf. [32]), as explained in [25], [27] and [28].

For instance, according to [25], an average-loss approach can be alternatively used to model the converter in Fig. 1(a), where the equivalent *switch resistances* denoted by R_{eq_i} are

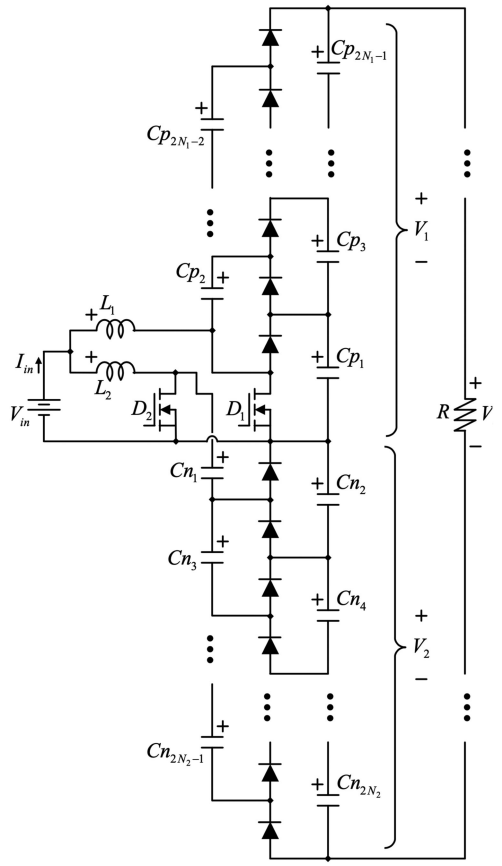

Fig. 2. Interleaved $N_1 + N_2$ multilevel boost converter.

explicitly used in the modeling process. By inspecting Fig. 1(a) the following set of equations are obtained as follows:

$$
\begin{aligned}
L\frac{d}{dt}i &= V_{\text{in}} - (1-D)V_{C_1}\\
C_1\frac{d}{dt}V_{C_1} &= (1-D)i - \frac{V_{C_1}-V_{C_2}}{R_{\text{eq1}}} - \frac{1}{R}\sum_{k-1}^{N} V_{C_{2k-1}}\\
C_2\frac{d}{dt}V_{C_2} &= \frac{V_{C_1}-V_{C_2}}{R_{\text{eq1}}} - \frac{V_{C_2}-V_{C_3}}{R_{\text{eq2}}}\\
C_3\frac{d}{dt}V_{C_3} &= \frac{V_{C_2}-V_{C_3}}{R_{\text{eq2}}} - \frac{V_{C_3}-V_{C_4}}{R_{\text{eq3}}} - \frac{1}{R}\sum_{k-1}^{N} V_{C_{2k-1}}\\
&\vdots\\
C_{(2N-2)}\frac{d}{dt}V_{C_{2N-2}} &= \frac{V_{2N-3}-V_{C_{2N-2}}}{R_{\text{eq}_{N-2}}} - \frac{V_{C_{2N-2}}-V_{C_{2N-1}}}{R_{\text{eq}_{N-1}}}\\
C_{(2N-1)}\frac{d}{dt}V_{C_{2N-1}} &= \frac{V_{C_{2N-2}}-V_{C_{2N-1}}}{R_{\text{eq}N-1}} - \frac{1}{R}\sum_{k-1}^{N} V_{C_{2k-1}}. \qquad (1)
\end{aligned}
$$

where the parameter N denotes the number of multiplier levels, and R_{eq_i} represent equivalent resistances inducing (average) losses due to the energy transfer among capacitors (see [25], [26] for further details). To avoid the use of such an excessive number of variables and equations, it is proposed to reduce the model order by assuming that every capacitance has the same value C, i.e., $C_i := C$, $i \in \{1, 2, \ldots\}$; and that the (average) voltage across capacitors is always the same. This approximation is justified by the self-voltage-balancing property of the converter (see [27] for further details), i.e., it is assumed that

$$V_o = \sum_{k-1}^{N} V_{C_{2k-1}}; \quad V_{C_1} \simeq V_{C_2} \simeq \cdots \simeq V_{C_{2N-1}}\,. \qquad (2)$$

As a result, the derivative of the voltage across the capacitors (that serve as energy transfer elements in Fig. 1, e.g., C_2 and C_{2N-2}) is equal to zero, i.e., the voltage across such capacitors is practically constant, which is a common assumption whenever the switching frequency is sufficiently high (see, e.g., [27]). Then, by adding up the equations of the output capacitor voltages, the following reduced-order model is obtained as follows:

$$
\begin{aligned}
L\frac{d}{dt}i &= V_{\text{in}} - (1-D)V_{C_1}\\
\sum_{k=1}^{N} C\frac{d}{dt}V_{C_{2k-1}} &= (1-D)i - \frac{1}{R}\sum_{k=1}^{N} V_{C_{2k-1}}. \qquad (3)
\end{aligned}
$$

By considering (2) and (3) can be expressed as follows:

$$
\begin{aligned}
L\frac{d}{dt}i &= V_{\text{in}} - \frac{(1-D)}{N}V_o\\
NC\frac{d}{dt}V_o &= (1-D)i - N\frac{V_o}{R}. \qquad (4)
\end{aligned}
$$

Notice that this model is similar to that of a conventional boost converter, i.e., for $N = 1$. Following the same considerations, a reduced-order model for the converter of Fig. 1(b) can be obtained. In fact, both models have identical structure. Consequently, an index term $j \in \{1, 2\}$ [$j = 1$ for Fig. 1(a) and $j = 2$ for Fig. 1(b)] is introduced to distinguish the effect of each model after the overall interleaved composed converter shown in Fig. 2. By adopting the notation of the general circuit in Fig. 2, then the overall model will remain for the rest of the article as follows:

$$
\begin{aligned}
L_j\frac{d}{dt}I_j &= V_{\text{in}} - \left(\frac{1-D_j}{N_j}\right)V_j\,, \quad j \in \{1,2\}\\
N_jC\frac{d}{dt}V_j &= (1-D_j)I_j - N_j\left(\frac{V_o}{R}\right) \qquad (5)
\end{aligned}
$$

where $I_{\text{in}} := I_1 + I_2$ represents the *total input current*, and $V_o := V_1 + V_2$ represents the total output voltage.

It can be easily verified that the total steady-state gain of the converter is given by

$$G := \frac{N_1}{1-D_1} + \frac{N_2}{1-D_2}\,. \qquad (6)$$

B. Sizing of the Inductors

One of the main interests while implementing interleaved converters is the mitigation of the input current ripple denoted by ΔI_{in}. This is usually achieved by a convenient switching coordination between the involved converters. For instance, a perfect ripple cancellation is achieved when using complementary duty cycles and complementary switching signals as those

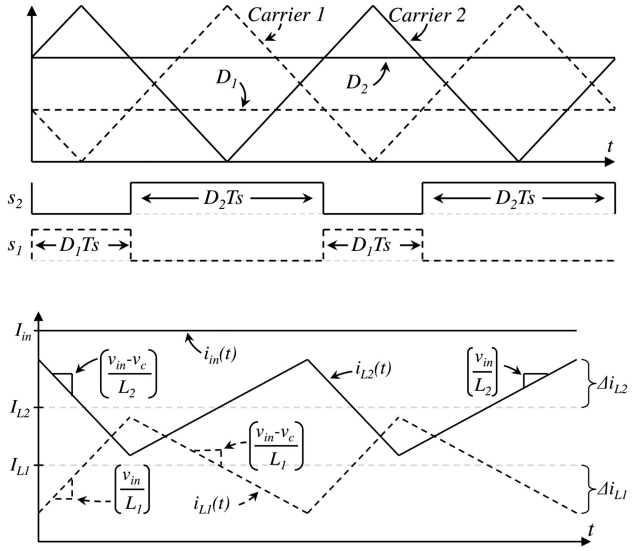

Fig. 3. Operating condition for total ripple cancellation.

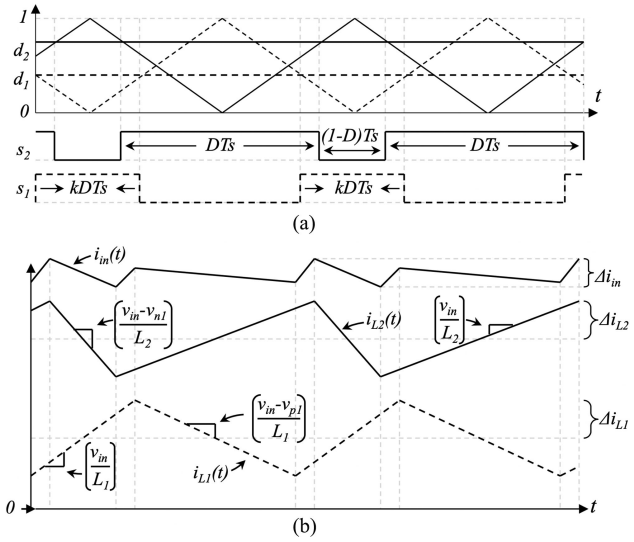

Fig. 4. PWM signals with overlapped switching functions.

shown in Fig. 3. In what follows, it is shown how this can be achieved for any desirable operating point provided an adequate inductors size specification.

The pulsewidth modulation (PWM) signals of the converters are generated by two triangular carriers, each of them associated with different duty cycles, see Fig. 3. The phase among triangular carriers as well as among firing signals is 180° degrees. In an ideal case, for a certain duty cycle, the input current ripple can be completely suppressed, this is shown in Fig. 3, in which $D_1 = (1 - D_2)$ and vice-versa.

In some cases, either the switching functions can be overlapped at certain values of duty cycles, or the value of duty cycle can produce dead times. The current waveforms corresponding to the former and the latter cases are illustrated in Figs. 4 and 5.

Consider the interleaved converter shown in Fig. 2. If the PWM carriers maintain a 180° phase shift with respect to

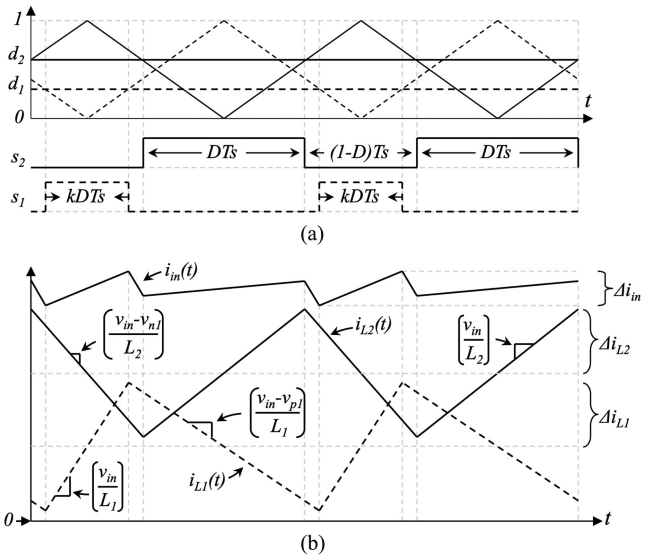

Fig. 5. PWM signals when switching functions are separated by a dead time.

each other, then the total current ripple can be computed as $\Delta I_{\text{in}} = \Delta I_1 - \Delta I_2$, i.e.,

$$\Delta I_{\text{in}} = \frac{V_{\text{in}} D_1}{2 f_s L_1} - \frac{V_{\text{in}} D_2}{2 f_s L_2} \,. \tag{7}$$

From (7), it can be noticed that in order to obtain $\Delta I_{\text{in}} = 0$ (perfect ripple cancellation), it is required either to constrain the values of duty cycles D_1 and D_2, which consequently will limit the gain of the converter (as usually done in traditional interleaved converters), or to design inductors L_1 and L_2 satisfying the following relation:

$$L_2 = L_1 \left(\frac{D_2}{D_1}\right) \,. \tag{8}$$

This allows to select any pair of arbitrary duty cycles and to compute the corresponding value of L_i, $i \in \{1, 2\}$. The latter yields a design approach that, first, does not restrict the gain of the converter and, second, allows a free selection of the operating point with $\Delta I_{\text{in}} = 0$. This idea has been exploited in [33] for an open-loop operation, and its advantage against traditional approaches is illustrated in Fig. 6. For example, there is not any restriction to select and deal with a gain induced by $D_2 = 0.713$, which may come out of a given specification. In general, there is a significant improvement in ripple cancellation around a selected operating region with different inductors, as compared to the current ripple obtained by traditional approaches.

In this article, this current ripple cancellation approach associated with the design of converters is the pivotal figure of the proposed MCRPT control technique. The following section provides the details of the closed-loop analysis.

IV. Current and Voltage Control Design

This section studies the dynamics of the converter for the design of stabilizing controllers.

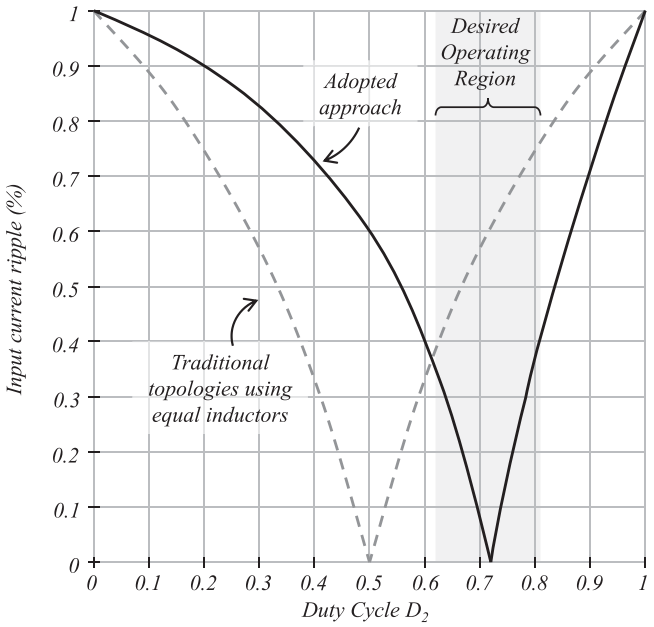

Fig. 6. Ripple level comparison under different design conditions.

A. Modeling Specification

As discussed in the previous section, the proposed converter is designed to operate under a fixed (but otherwise arbitrary) operating region, for which the input current ripple is minimized. Hence, we use the linear version of the model in (5) in order to design controllers able to guarantee stability and performance over such desired region. The model is now formulated in terms of incremental variables in state-space form, which yields

$$\frac{d}{dt}\begin{bmatrix}\Delta I_j\\ \Delta V_j\end{bmatrix} = \underbrace{\begin{bmatrix}0 & \frac{(1-\overline{D}_j)}{N_j L_j}\\ \frac{(1-\overline{D}_j)}{N_j C} & \frac{N_j}{RC_j}\end{bmatrix}}_{=:A_j}\begin{bmatrix}\Delta I_j\\ \Delta V_j\end{bmatrix} + \underbrace{\begin{bmatrix}\frac{\overline{V}_j}{N_j L_j}\\ \frac{-\bar{i}_j}{C}\end{bmatrix}}_{=:B_j}\Delta D_j \tag{9}$$

where $\Delta I_j := I_j - \bar{i}_j$ is the incremental value of the variable I_j, with respect to its desired value $\bar{i}_j$ at steady state, with $j = 1, 2$. The rest of the variables are thus defined analogously.

B. Input Current and Output Voltage Control

The controller must guarantee regulation of the output voltage toward a constant or variant reference. However, it is well-known that boost converters have a *nonminimum phase characteristic* with respect to the output voltage, i.e., the corresponding duty cycle-to-voltage transfer function has a zero in the right half plane. This situation implies a reduction on the controller bandwidth, which limits the parametric selection of closed-loop gains (see [34, Sec. 5.6]) and acts as a potential instability mechanism (see [32], [35]). An alternative, which is usual in practice, consists in indirectly regulate the output voltage by directly regulating the inductor current which is of minimum phase.

The input current control loop is implemented by the following *PI controllers* for both converters:

$$\Delta D_j := -k_{j,1}x_j - k_{j,2}\Delta I_j;\quad j = 1, 2 \tag{10}$$

where $k_{j,1}$, $k_{j,2}$ are the controller gains; x_j, is the integral of the error of the variable ΔI_j with respect to a reference $i_{\text{ref},j}$, $j = 1, 2$; and whose state-space equation is given by

$$\frac{d}{dt}x_j = \Delta I_j - i_{\text{ref},j};\quad j = 1, 2\,. \tag{11}$$

The output-voltage loop is analogously defined in a nested form in order to ensure voltage stabilization at the desired operating point, i.e.,

$$i_{\text{ref},j} := -g_{j,1}z_j - z_{j,2}\Delta V_j;\quad j = 1, 2 \tag{12}$$

where $g_{j,1}$ and $g_{j,2}$ are the controller gains, and z_j, $j = 1, 2$, is the integral of the error variable $\Delta V_j = V_j - \overline{V}_j$ with respect to zero; or equivalently the integral of the error between the voltage V_j and its desired reference $\overline{V}_j$, $j = 1, 2$; and whose state-space equation is given by

$$\frac{d}{dt}z_j = \Delta V_j = V_j - \overline{V}_j;\quad j = 1, 2\,. \tag{13}$$

C. Controller Gain Tuning to Ensure Stability

Once the controller scheme has been proposed, the controller gains are tune to guarantee stability in terms of a set of LMIs derived from the *Lyapunov stability theorem* (see [36], Section 7.4).

Using (9) and the controller (10), (11) and (12), (13), the model can be reformulated with an extended state space as follows:

$$\frac{d}{dt}\begin{bmatrix}\Delta I_j\\ \Delta V_j\\ x_j\\ z_j\end{bmatrix} = \underbrace{\begin{bmatrix}A_j - k_{j,2}B_j[1\ \ 0] & -k_{j,1}B_j & 0_{2\times 1}\\ [1\quad g_{j,2}] & 0 & g_{j,1}\\ [0\quad 1] & 0 & 0\end{bmatrix}}_{=:\widetilde{A}_j}\begin{bmatrix}\Delta I_j\\ \Delta V_j\\ x_j\\ z_j\end{bmatrix} \tag{14}$$

with $j = 1, 2$; hence the closed-loop system can be represented by the matrix $\widetilde{A}_j$. As stated in [36, Theorem 7.4.4, pp. 263–264] this closed-loop system is asymptotically stable if there exists a matrix $P_j > 0$, $j = 1, 2$, of suitable size such that

$$Q_j := \widetilde{A}_j^{\top}P_j + P_j\widetilde{A}_j < 0;\quad j = 1, 2. \tag{15}$$

Since the parameters of both P_j and $\widetilde{A}_j$ (the controller gains) are unknown, condition (15) is a bilinear matrix inequality, for which iterative algorithms can be employed to find suboptimal solutions (see [37]). This is actually a straightforward matter for solvers such as `Yalmip`.

Since the inequality (15) provides a family of solutions corresponding to different left-half plane eigenvalues and consequently different time constants; we now provide a way to characterize all solutions. This is possible since according to [38, Theorem 3.3], there exists a positive constant ϵ_j such that

$$Q_j - 2\epsilon_j P_j < 0;\quad j = 1, 2. \tag{16}$$

Since $P_j > 0$, then it can be factorized as $P_j := N_j^\top N_j$, where N_j is square and nonsingular. Consequently, inequality (16) can be written as

$$N_j^{-T} Q_j N_j - 2\epsilon_j I < 0; \quad j = 1, 2 \tag{17}$$

Hence, $\epsilon_j < -\frac{1}{2}\lambda_{\max}$, where $-\lambda_{\max}$ is the largest eigenvalue of $N_j^{-T} Q_j N_j$, $j = 1, 2$ in (17). Consequently, ϵ_j must necessarily belong to an interval $[0, -\frac{1}{2}\lambda_{\max}]$. In short, by modifying the value of ϵ, we obtain different solutions of (15) from which we can chose the most suitable time constant for A_j, $j = 1, 2$, according to our desired dynamic response.

V. Minimum Current Ripple Point Tracking

The control set-up, introduced in the previous section, can be used to implement any technique currently available in the literature for interleaved converters, e.g., current balancing, equal, or complementary duty cycles, etc. We now introduce an additional control law that is able to guarantee input current minimization. This is in sharp contrast with the rest of the schemes whose operating point cannot be freely chosen and whose controller does not minimize the current ripple when the converters deviate from such point.

This strategy is called *MCRPT* technique. Based on the findings presented in Section III-B, it is proposed an implementation that adds additional constraints to the controllers introduced in Section IV, i.e., to achieve input current stabilization and output-voltage control, while featuring the least possible percentage of input current ripple at any operating point.

This technique can be applied to any interleaved topology with dual input switched inductors, i.e., converters with the following.

1) Two input inductors controlled by different switches.
2) Switches are able to adopt different duty cycles.

This is the case of plenty of emerging topologies (see, e.g., the case of double dual boost converters [17], [22] and the compendium of topologies included as a review in [23].

Based on this premises, we consider an interleaved converter whose inductances have a relationship given in (8), and whose PWM carriers are in counter phase. This yields the following relationship:

$$k := \frac{L_1}{L_2} = \frac{D_1}{D_2}. \tag{18}$$

The concept of MCRPT follows from (18), which establishes the following duty cycle relationship:

$$D_1 = kD_2. \tag{19}$$

Fig. 7 depicts curves that show the zero ripple points in terms of the design parameter k, and how the ripple level increases when the operating point moves away. Notice that the small amount of ripple on the input current is an advantage that follows the design of the converter according to a preselected minimum ripple point, while the condition (19) can be satisfied via an active MCRPT technique that "chases" the curve.

For the MCRPT application, an additional controller is considered to link both multilevel converter controllers to guarantee output voltage regulation, plus an additional condition

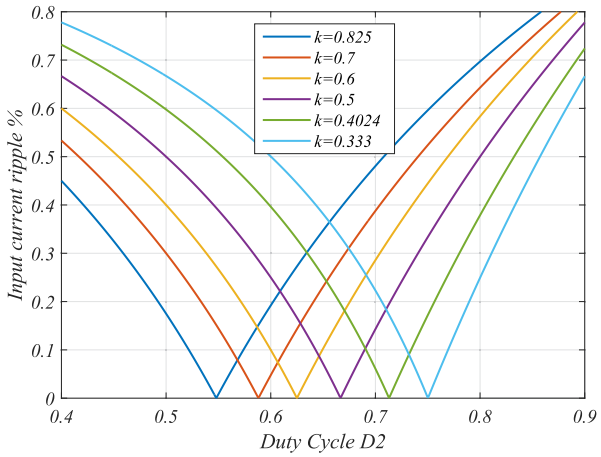

Fig. 7. MCRPT curves according to inductors relationship, i.e., curves of input ripple as a function of the duty cycle for different values of k.

satisfying (19). To implement the MCRPT scheme (the third stage), the following control law is introduced:

$$\frac{d}{dt} w = D_1 - kD_2 \tag{20}$$

where w is a variable that implements the, so called, MCRPT. The following additional term is introduced to the output-voltage loops as follows:

$$\begin{aligned} i_{\text{ref}_1} &= -g_{1_1} V_1 - g_{2_1} z_1 + g_3 w \\ i_{\text{ref}_2} &= -g_{1_2} V_2 - g_{2_2} z_2 - g_3 w. \end{aligned} \tag{21}$$

Notice that, based on (21), the currents set-points are function of both the output voltages and w. The MCRPT law steers the duty cycles to a point that satisfies condition (19).

The rationale behind the proposition of (20) is the accomplishment of condition (19), which is possible in steady state [(20) becomes (19)] as long as the gain g_3 is suitably selected in such a way that the whole closed-loop system is asymptotically stable. In order to guarantee such stable operation, we can simply further extend the models (22) by including (20), which yields

$$\frac{d}{dt}\begin{bmatrix} \Delta I_1 \\ \Delta V_1 \\ x_1 \\ z_1 \\ \Delta I_2 \\ \Delta V_2 \\ x_2 \\ z_2 \\ w \end{bmatrix} = \underbrace{\begin{bmatrix} \widetilde{A}_1 & 0_{4\times 4} & \begin{bmatrix} 0 \\ -g_3 \\ 0_{2\times 1} \end{bmatrix} \\ 0_{4\times 4} & \widetilde{A}_2 & \begin{bmatrix} 0 \\ g_3 \\ 0_{2\times 1} \end{bmatrix} \\ \widetilde{D}_1 & -k\widetilde{D}_2 & 0 \end{bmatrix}}_{=:\widetilde{A}} \begin{bmatrix} \Delta I_1 \\ \Delta V_2 \\ x_1 \\ z_2 \\ \Delta I_1 \\ \Delta V_2 \\ x_1 \\ z_2 \\ \end{bmatrix} \tag{22}$$

where

$$\begin{aligned} \widetilde{D}_1 &:= [-k_{1,2} \;\; 0 \;\; -k_{1,1} \;\; 0] \\ \widetilde{D}_2 &:= [-k_{2,2} \;\; 0 \;\; -k_{2,1} \;\; 0]. \end{aligned}$$

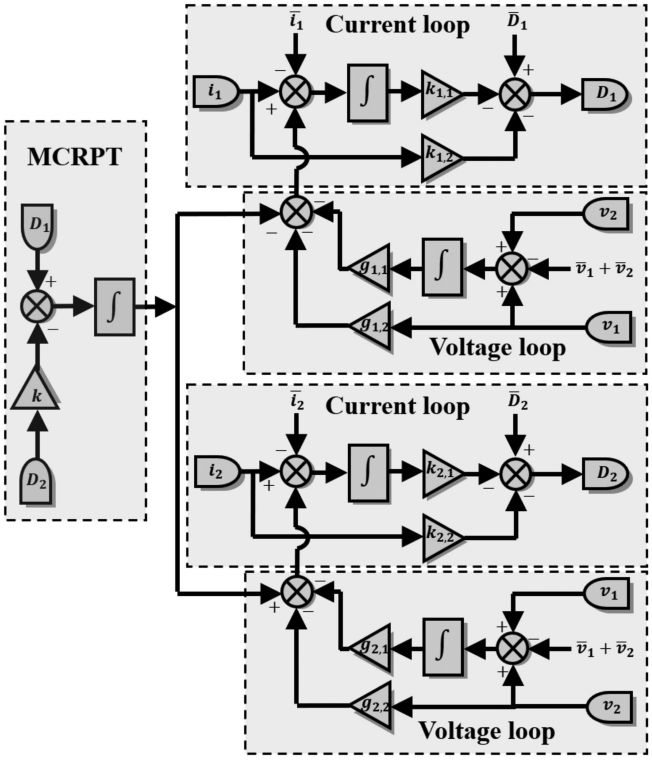

Fig. 8. Proposed control strategy encompassing current/voltage loops and MCRPT.

Note that an important implication of (22) is that the resulting full closed-loop system (including the MCRPT loop) is *autonomous*. This means that the future of the system is completely determined by its past, i.e., the system is *causal* (see [36, Sec. 3.2]). Consequently, although the duty cycles are involved in the computation of the control law, its implementation can be carried out as in any other traditional closed-loop controller, where current initial conditions are used to compute future input values.

Finally, the full set of gains can be computed in an analogous way as in Section IV, i.e., by finding a matrix $P > 0$ of suitable size, such that

$$Q := \widetilde{A}^\top P + P\widetilde{A} < 0\,. \tag{23}$$

which can be easily done by using `Yalmip`. Finally, we illustrate the the full schematic of the controller in Fig. 8.

A. Other Configurations: Current Control and MPPT

In some cases, we might be interested in the combination of the MCRPT technique with a MPPT algorithm, as in the case of photovoltaic systems. In this case, any MPPT can be used. The diagram in Fig. 8 is simplified to adopt a current control mode. The current control is thus driven by the selected MPPT technique while maintaining the same rationale of gain computation. The resulting configuration is illustrated in Fig. 9.

Note that both *voltage regulation* (see Fig. 8) and *MPPT* (see Fig. 9) act upon a current controller, as well as the proposed

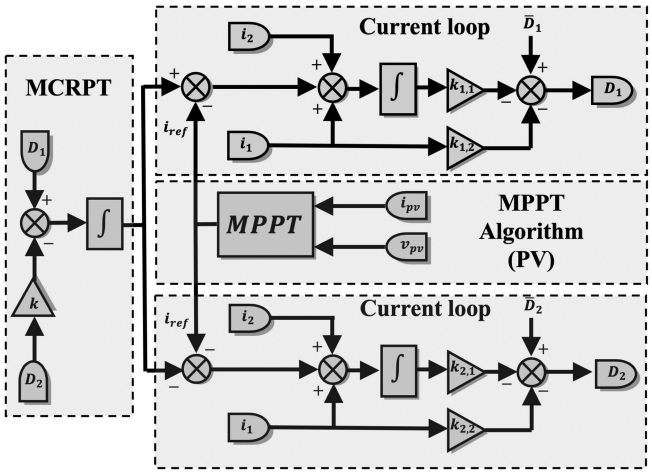

Fig. 9. Proposed MCRPT control strategy simultaneously operating with any suitable maximum power point tracking (MPPT) technique for a photovoltaic system with current i_{pv} and voltage v_{pv}.

TABLE I
PARAMETERS OF THE EXPERIMENTAL SETUP

Parameter	*Value*
L_1	$237\ \mu H$
L_2	$90\ \mu H$
C	$10\ \mu F$
Mosfets	$IRFP250$
Diodes	*BYW29E-400*
Resistance	$500\ \Omega$
N_1, N_2	2
PWM frequency	$50kHz$
ADC sampling	$200kHz$
Integration step	$5\mu s$
V_{in}	$24\ V$
V_{out}	$192\ V$
$k = L_1/L_2$	2.633
$\overline{D}_1,\ \overline{D}_2$	0.627,0.238
$\overline{V}_1,\ \overline{V}_2$	128.97V, 63.02V
$\overline{I}_1,\ \overline{I}_2$	2.06A, 1A

MCRPT control. Consequently, it is possible to interchange objectives that define a current reference without conflict.

VI. EXPERIMENTAL SETUP AND VALIDATION

The proposed controller was validated using an experimental prototype of a four-level version of the converter in Fig. 2, i.e., $N_1 = 2$ and $N_2 = 2$. It comprises an electronic load at the output and a digital signal processor TI TMS320F28335 as the control platform. The parameters of the converter as well as other useful information about the implementation are shown in Table I.

In order to avoid compromising the stability properties and the performance of the controller that were achieved in the theoretical analysis, it must be guaranteed that the *Nyquist*

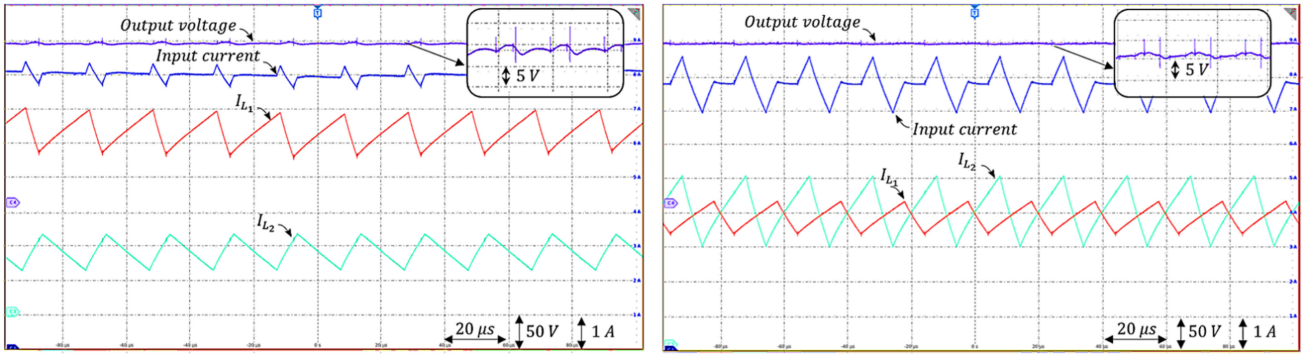

Fig. 10. Experimental results at $V_{\text{in}} = 20$ V of input current ripple cancellation using the proposed MCRPT (left) and without it, by applying traditional current balancing (right).

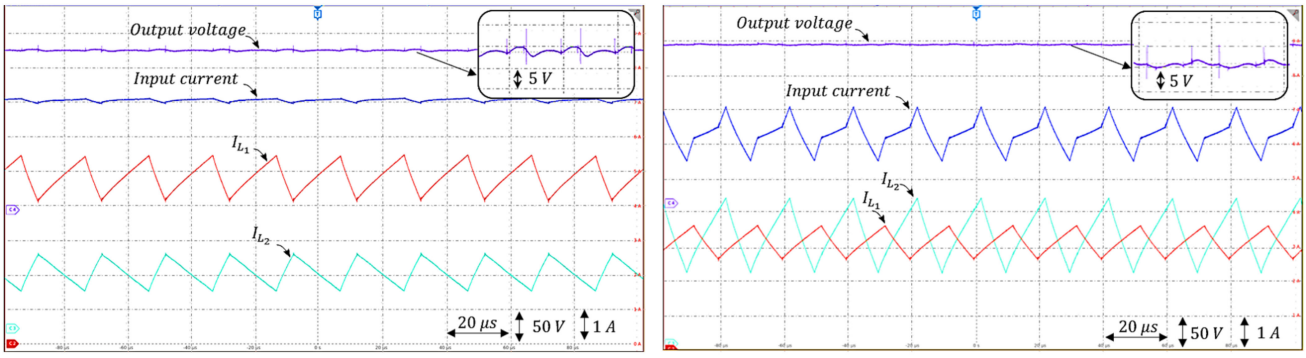

Fig. 11. Experimental results at $V_{\text{in}} = 24$ V of input current ripple cancellation using the proposed MCRPT (left) and without it, by applying traditional current balancing (right).

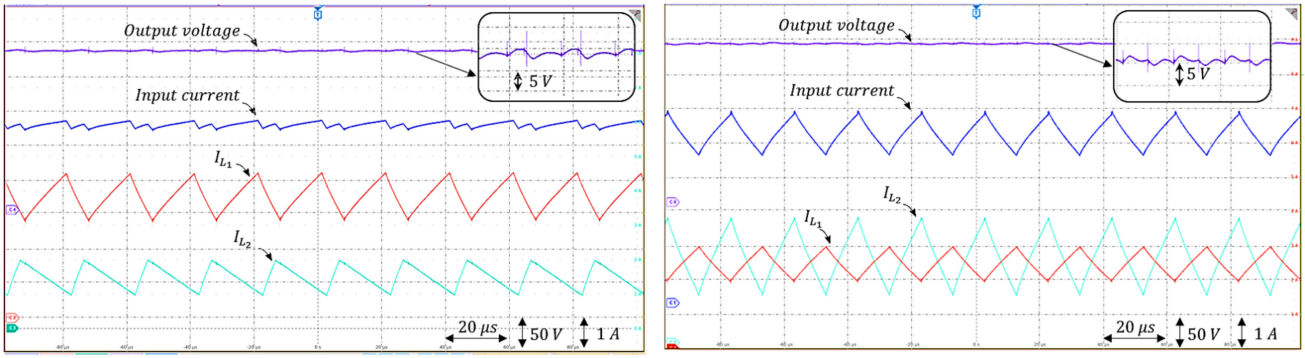

Fig. 12. Experimental results at $V_{\text{in}} = 30$ V of input current ripple cancellation using the proposed MCRPT (left) and without it, by applying traditional current balancing (right).

frequency criterion is satisfied, namely, that the continuous-time signals are sampled at a frequency that is at least twice the value of the switching frequency (see [39, Sec. 2.2]). In this case, the digital signal processor set-up permits a sample frequency equal to 100 kHz, i.e., twice the switching frequency. The controller gains were obtained by solving the inequality (23) using `Yalmip`. The controller gains used in this work are: $k_{1,1} = 0.198$, $k_{1,2} = 0.112$, $g_{1,1} = 18$, $g_{1,2} = 18.8$, $k_{2,1} = 0.038$, $k_{2,2} = 0.012$, $g_{2,1} = 3.5$, $g_{2,2} = 6.3$, and $g_3 = 1100$.

As previously stated, the main advantage of the presented controller is its ability to reach an operating point such that the minimum ripple condition is guaranteed, while preserving voltage regulation. For validation purposes, a controller featuring the traditional approach, namely, current balancing (cf., [7]–[9]) is implemented and compared with the propose MCRPT controller using the same converter. To corroborate that the proposed MCRPT control strategy always achieves minimum ripples, the topology is operated under variations of the input voltage: 20 V, 24 V, 30 V, which involves a significant change in the input current due to the high voltage gain of the converter. The results are shown in Figs. 10–12. The experimental results also contain the output voltage ripple to corroborate that it is

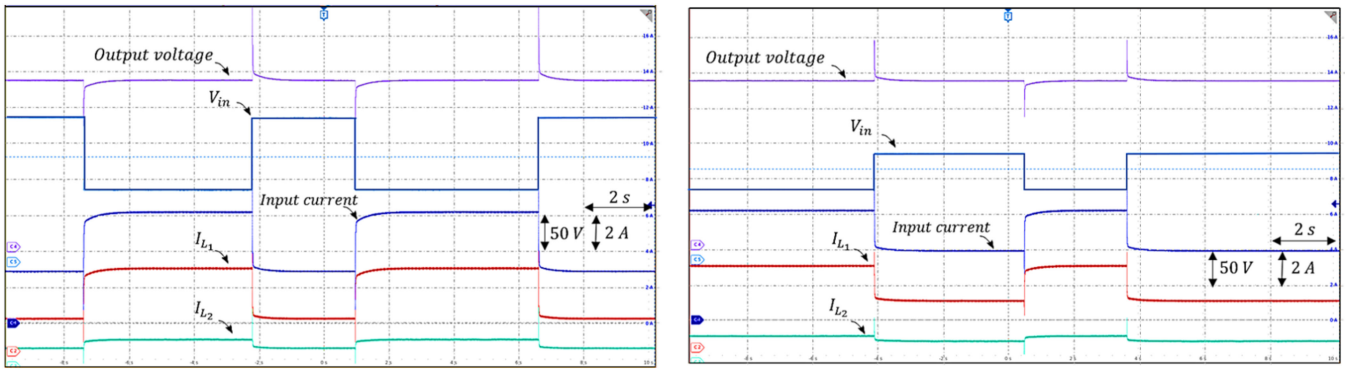

Fig. 13. Dynamical response of the MCRPT under abrupt variations on the input voltage: 20–40 V and vice versa (left) and 30–40 V and vice versa (right).

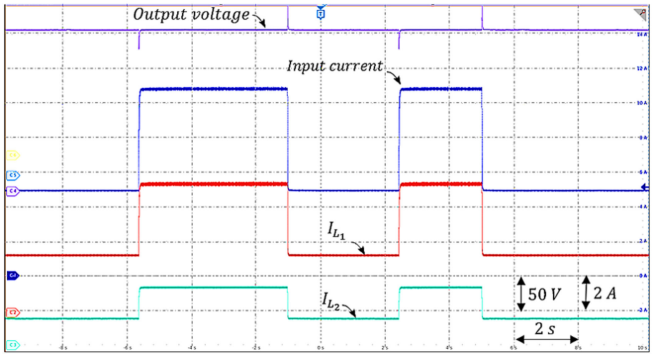

Fig. 14. Dynamical response of the MCRPT under abrupt variations on the output load from 45 to 100% and vice versa.

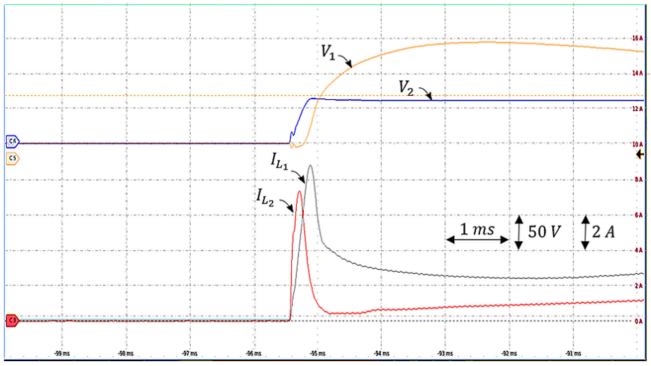

Fig. 15. Dynamic response from zero initial conditions.

not affected by the current ripple cancellation technique. Notice that although both controllers achieve the same output voltage 200 V, only the MCRPT is able to minimize the current ripple by searching for the minimum ripple condition $D_1 = kD_2$, despite of input voltage changes.

In Fig. 13, we show the full dynamics of the converter to validate its robustness of the output voltage regulation against continuous variations in the input voltage between 20 V– and 40 V and 20 V– and 30 V. Moreover, the robustness of the MCRPT algorithm to search the optimal current ripple cancellation condition. Notice that the steady-state traces (zooming in) correspond to the results previously shown in of the steady-state experiments previously shown in Figs. 10–12. Finally, Fig. 14 depicts experimental results show that the dynamical response of the converter with respect to abrupt load changes. We start with a nominal value $R = 400\ \Omega$ and then we change repeatedly to $180\ \Omega$ and 400Ω, which corresponds to variations of 45 to 100% of nominal load and vice versa.

In order to show the dynamic performance of the converter, we present the initial transient from zero initial conditions with an output voltage set point equal to 200 V and an input voltage equal to 24 V, see Fig. 15.

VII. Conclusion

In this article, a MCRPT control scheme was proposed. Such control law contains a correction term that gradually deviates the operating point of duty cycles toward a point where minimum input current ripple can be achieved. That is, a new approach was adopted to guarantee current ripple cancellation for which duty cycles were not constrained as in the strategies currently available in the literature. We showed that the active minimum input current ripple point tracking implementation permits a minimum current-ripple despite of a variable operating point. Experimental results showed that the proposed scheme was able to simultaneously achieve input current stabilization, output voltage regulation and input current ripple minimization despite of disturbances such as input voltage and load changes.

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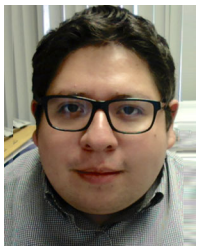

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Chapter 3

Discrete-time Modeling and Control of Double Dual Boost Converters with Implicit Current-Ripple Cancellation over a Wide Range Operating Range

Summary of the chapter

This chapter introduces discrete-time controllers for double dual boost converters in, that are suitable for renewable energy applications. The proposed schemes are based on a current ripple mitigation technique, which enables an unconstrained input-to-output voltage converter gain. This is in contrast with classical interleaved topology implementations, where duty cycles are restricted (e.g. to 50%). A discrete-time small-signal controller is proposed for those applications that require nominal specifications. This control strategy is based on a novel linear difference system approach, while gain tuning is performed via numerical computation of linear matrix inequalities (LMIs). In addition, a discrete-time large-signal controller is proposed for those applications that require trajectory tracking. The proposed controllers, their stability, performance and ripple cancellation properties are validated via experimental results.

Discrete-Time Modeling and Control of Double Dual Boost Converters With Implicit Current Ripple Cancellation Over a Wide Operating Range

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***Abstract*—This article introduces discrete-time controllers for double dual boost converters, suitable for renewable energy applications. The proposed schemes are based on a current ripple mitigation technique, which enables an unconstrained input-to-output voltage converter gain. This is in contrast with classical interleaved topology implementations, where duty cycles are restricted (e.g., to 50%). A discrete-time small-signal controller is proposed for those applications that require nominal specifications. This control strategy is based on a novel linear difference system approach, whereas gain tuning is performed via numerical computation of linear matrix inequalities. In addition, a discrete-time large-signal controller is proposed for those applications that require trajectory tracking. The proposed controllers, their stability, performance, and ripple cancellation properties are validated via experimental results.**

***Index Terms*—DC–DC converters, discrete-time control, double dual boost converter, interleaved converters, ripple cancellation.**

I. Introduction

COMMONLY, renewable energy systems require a dc–dc conversion stage to step up the generated voltage, as a preamble for dc–ac conversion for grid integration. Consequently, boost-type converters are often implemented [1]. In this type of applications, the input current ripple of the dc–dc converters is undesirable, since it produces a negative impact on renewable energy sources (e.g., solar panels and fuel cells), in terms of their lifetime and efficiency [2]–[4].

Consequently, the development of input current ripple cancellation techniques has become a very active research field in the last years, reporting a significant number of contributions [5]–[12]. In [5], Mazumder *et al.* used a filter based on coupled inductors to deal with this issue. In [6], an interleaved structure was combined with coupled inductors. Unfortunately, coupled inductors require a tailored design, which undermines the use of off-the-shelf components. In [7], Rana *et al.* proposed a tristate boost converter to improve the dynamical performance. However, the input current ripple is higher in comparison with an interleaved converter. In [8], a linear controller was designed to induce ripple cancellation. However, a restriction of equal duty cycles limits the operation of the converter due to a fixed voltage gain. This is not a sheer coincidence, since literature in interleaved topologies shows a common inclination to the use of restrictive duty cycles; consequently, the converter gain is restricted by the topology, not by the application requirements, see, e.g., [13]–[15]. For instance, if a different gain is required, then the topology is typically modified by adding more switched inductor phases, see, e.g., [16]. In [10], Soriano-Rangel *et al.* proposed an improvement for the technique presented in [9], where an unconstrained duty cycle relationship is presented. However, this novel condition is only devised for open-loop stand-alone implementations.

Among current trends, the use of interleaved converters is identified as a highly suitable choice to mitigate input current ripples, see, e.g., [7]–[12]. However, there is still significant room for improvement in terms of unconstrained operation, i.e., free selection of voltage gain and closed-loop implementations. Control design of dc–dc converters is usually carried out by considering continuous-time variables. This is a common practice, since the assumption of continuous-time facilitates the development of control strategies, although a digital implementation is usually required anyway. On the other hand, despite the fact that control design analysis might be more involving in discrete time, it permits to obtain a reduced computational cost, in terms of sampling frequencies [17]. Moreover, we are able to bypass

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the requirement of numerical integration, which is replaced by recursive easy-to-implement summations [18]–[20].

In some applications, closed-loop dc–dc converters are designed to operate under nominal conditions, i.e., a fixed operation point is required (e.g., voltage regulation). Consequently, this has motivated the use of a *small signal approach*, which enables powerful tools of linear control design, such as frequency domain analysis, robust control, convex optimization, etc., see, e.g., [21]–[23]. On the other hand, some applications require a variable operating region, e.g., the implementation of maximum power point tracking schemes, where currents and voltages vary over a relatively large range. In this case, a *large-signal approach* can be of interest, which involves nonlinear control [24].

Motivated by the aforementioned trends in high-gain and current ripple cancellation topologies and their control, we introduce novel digital control strategies for *interleaved double dual boost converters* [8]. We introduce both, a small-signal (linear) and a large-signal (nonlinear) settings that can cover a wide application of modern scenarios that require high-voltage gains and current ripple cancellation. These strategies include an *implicit* condition to current ripple mitigation, that permits to arbitrarily select the converter gain, which is in contrast with the current state of the art. This condition is based on the application of an inductance ratio and a new modeling specification for the converter. Then, a closed-loop implementation is performed directly in discrete-time terms.

II. Models of Power Converter Dynamics

In this section, we examine several approaches to power converter modeling. These models, in particular those in discrete time, will be instrumental for the development of the control strategies developed in this article.

A. Continuous-Time Piecewise Linear Dynamics

DC–DC converters exhibit *piecewise linear trajectories* of voltages and currents. For simplicity, we often consider that dynamics are generated by two modes (ON/OFF), constant inputs, and ideal switches. Then, we can use the following structure:

$$\frac{d}{dt}x = A_j x + B_j \; ; \; j = 1, 2 \tag{1}$$

where $x(t) \in \mathbb{R}^n$ is called state function; $A_j \in \mathbb{R}^{n\times n}$ and $B_j \in \mathbb{R}^{n\times 1}$, with $j = 1, 2$, are matrices that describe the physical laws of the dynamic modes.

A switching signal $s : \mathbb{R} \to \{1, 2\}$ determines the value of j, which is an index term that denotes which of the two modes is active due to the position of diodes and transistors.

A traditional *pulsewidth modulation* is based on a periodical switching signal defined as

$$s(t) : \begin{cases} j = 1, & t_k \le t < t_k + dT \\ j = 2, & t_k + dT \le t < t_k + T \end{cases} \tag{2}$$

with $t_0 := 0$, $t_{k+1} = t_k + T$, $k = 0, 1, 2, \ldots$; where $d \in [0, 1]$ is called *duty cycle* and T is the *switching period*. In this article, we use the ":=" to denote a definition.

B. Continuous-Time Large-Signal and Small-Signal Dynamics

We can *approximate* the instantaneous piecewise linear dynamics of the converter into "average" ones, by involving the duty cycle in the description of the system (1). The *averaging technique* yields the following structure:

$$\frac{d}{dt}x = \underbrace{[dA_1 + (1-d)A_2]\, x + dB_1 + (1-d)B_2}_{=:f(x,d)} \tag{3}$$

where $x(t) \in \mathbb{R}^n$ is an *averaged state function*.[1] This modeling specification is predominant in the analysis of power converters (cf., [25]). Common names include average model, nonlinear/large-signal model, and small-ripple approximation.

Typically, converters are designed according to nominal specifications, i.e., they work around a bounded operating region. For this reason, *small-signal models* (cf., [25]) become of interest. These models permit to represent the dynamics of the system in an accurate way while enabling linear tools for control design and optimization [24]. A small-signal model can be obtained from (3) by defining a nominal (equilibrium) specification for the state and the duty cycle, i.e., $(\overline{x}, \overline{d})$. Then, incremental variables, $\Delta x := x - \overline{x}$ and $\Delta d := d - \overline{d}$, are used to obtain

$$\frac{d}{dt}\Delta x = \overline{\mathbf{A}} \cdot \Delta x + \overline{\mathbf{B}} \cdot \Delta d \tag{4}$$

where

$$\overline{\mathbf{A}} := \left.\frac{\partial f(x,d)}{\partial x}\right|_{x=\overline{x},\, d=\overline{d}.}, \quad \overline{\mathbf{B}} := \left.\frac{\partial f(x,d)}{\partial d}\right|_{x=\overline{x},\, d=\overline{d}.}.$$

This description is called *small-signal continuous-time model.*

C. Discrete-Time Small-Signal Model

The linear model (4) admits *exact discretization* (cf., [17]), with respect to a sampling period h. Since the time-domain solution of the state-space system (4) is given by

$$\begin{aligned} \Delta x(t) &= e^{\overline{\mathbf{A}}t} \cdot \Delta x(0) + \int_0^t e^{\overline{\mathbf{A}}(t-\tau)}\overline{\mathbf{B}} \cdot \Delta d(t) d\tau \\ &= e^{\overline{\mathbf{A}}t} \cdot \Delta x(0) + \overline{\mathbf{A}}^{-1}(e^{\overline{\mathbf{A}}h} - I)\overline{\mathbf{B}} \cdot \Delta d(t) \end{aligned} \tag{5}$$

then assuming that h is small enough, such that the values of Δx and Δd remain about constant, we obtain

$$\Delta x(h) = e^{\overline{\mathbf{A}}h} \cdot \Delta x(0) + \overline{\mathbf{A}}^{-1}(e^{\overline{\mathbf{A}}h} - I)\overline{\mathbf{B}} \cdot \Delta d(0) \; .$$

This equation can be generalized for any arbitrary sampling time $t_i \in \mathbb{R}$, and initial condition $x(t_i)$, with $t_{i+1} = t_i + h$, $i = 1, 2, 3, \ldots$. This yield

$$\Delta x(t_{i+1}) = e^{\overline{\mathbf{A}}h} \cdot \Delta x(t_i) + \overline{\mathbf{A}}^{-1}(e^{\overline{\mathbf{A}}h} - I)\overline{\mathbf{B}} \cdot \Delta d(t_i) \; .$$

Finally, we can formulate the following small-signal state-space model:

$$\sigma \Delta x = \overline{\mathbf{F}} \cdot \Delta x + \overline{\mathbf{G}} \cdot \Delta d \tag{6}$$

[1]For ease of exposition, in this article, we adopt the same notation for x in continuous/discrete piecewise/average domains, whereas the elements and operators in the model permit to avoid ambiguity.

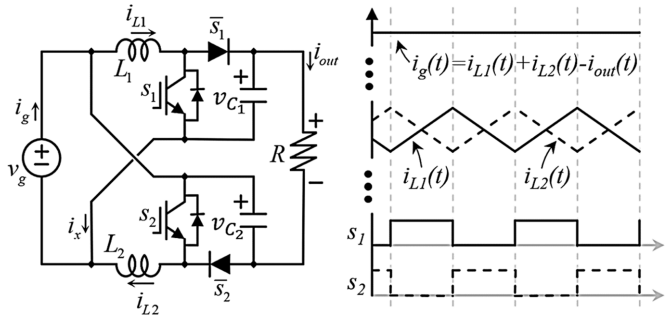

Fig. 1. Double dual boost converter topology.

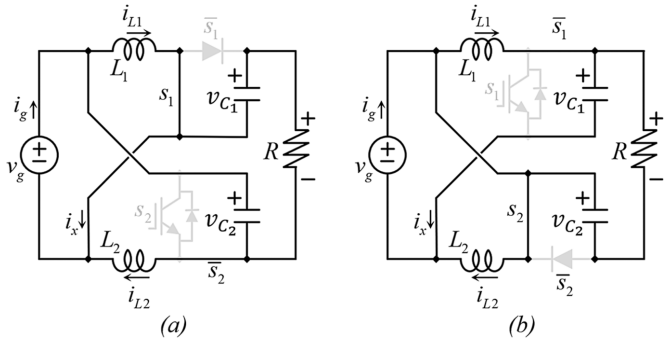

Fig. 2. Double dual boost converter switching states.

where the incremental state and duty cycle are now discrete-time functions, i.e., $\Delta x : \mathbb{N} \to \mathbb{R}^n$ and $\Delta d : \mathbb{N} \to \mathbb{R}$; σ denotes the shift operator acting on $\Delta x(t_i)$, defined as $\sigma x(t_i) := \sigma x(t_{i+1})$; and $\overline{\mathbf{F}} := e^{\overline{\mathbf{A}}h}$, $\overline{\mathbf{G}} := \overline{\mathbf{A}}^{-1}(e^{\overline{\mathbf{A}}h} - I)\overline{\mathbf{B}}$.

D. Discrete-Time Large-Signal Model

In some cases, power converters are designed to operate on different operating points, then large-signal models are of interest to model a dynamic behavior over wide variations of voltages, currents, and duty cycle. We can construct a model via *approximate discretization* based on a continuous-time average model. Using the elements of (3), define $A_d := dA_1 + (1-d)A_2$ and $B_d := dB_1 + (1-d)B_2$. Then, by following an analogous procedure as in (5), we obtain the following time-domain model:

$$x(t) = e^{A_d t} \cdot x(0) + {A_d}^{-1}(e^{A_d t} - I)B_d \ .$$

Considering every solution of the aforementioned equation with respect to a small sample time h, an equation analogous to (6) can be hence expressed as

$$\sigma x = e^{A_d h}x + {A_d}^{-1}(e^{A_d h} - I)B_d \ . \tag{7}$$

Finally, by considering the approximation $e^{A_d h} \approx I + A_d h$, which correspond to the most significant components of an infinite Maclaurin series; and after straightforward algebraic manipulations, the following large-signal discrete-time model is obtained:

$$\sigma x = (I + A_d h)x + B_d h \ . \tag{8}$$

In the following sections, linear (small-signal) and nonlinear (large-signal) controllers are designed to guarantee a constant output voltage, despite abrupt variations on the load, the input-voltage and the desired set-point.

III. Classic Operation and Steady-State Analysis of Double Dual Boost Converters

In this section, the main properties of the double dual boost converter [8] are examined. The topology and a typical input current operation are depicted in Fig. 1. The traditional approach consist in the use of complementary duty cycles whose carriers have 180° phase shift. In this standard setting, the point of perfect cancellation occurs when the duty cycle of each transistor holds $d := d_1 = d_2 = 0.5$. This is the common practice for this and other similar topologies (see, e.g., [8], [13]–[16]).

The input current is equal to the sum of both inductor currents minus the output current. This can be observed in Fig. 1, from the reference node of the input power source, $i_g = i_x + i_{L_2}$. The current i_x comes from a supernode comprised by the transistor and diode S_1 and $\overline{S}_1$, and capacitor C_1. From this supernode, $i_x = i_{L_1} - i_{\text{out}}$. Then, the input current can be expressed as $i_g = i_{L_1} + i_{L_2} i_{\text{out}}$. During the traditional operation, duty cycles are complementary. This allows to achieve perfect input current ripple cancellation with duty cycles at 50%, though as argued afterward, this is not the only condition to achieve ripple cancellation.

To analyze the topology at steady state, continuous conduction mode (CCM) is considered. The components are designed in such a way that the ripple can be neglected, which allows to consider an average analysis as in (3). The ON/OFF operation modes of the converter are shown in Fig. 2.

An instantaneous (piecewise linear) model as in (1) is obtained by defining $x^\top := [i_{L_1} \quad v_{C_1} \quad i_{L_2} \quad v_{C_2}]\top$, with the matrices

$$A_1 = \begin{bmatrix} 0 & 0 & 0 & 0 \\ 0 & \frac{-1}{RC_1} & 0 & \frac{-1}{RC_1} \\ 0 & 0 & 0 & \frac{-1}{L_2} \\ 0 & \frac{-1}{RC_2} & \frac{1}{C_2} & \frac{-1}{RC_2} \end{bmatrix}, \quad B_1 = \begin{bmatrix} \frac{1}{L_1} \\ \frac{1}{RC_1} \\ \frac{1}{L_2} \\ \frac{1}{RC_2} \end{bmatrix} v_g$$

$$A_2 = \begin{bmatrix} 0 & \frac{-1}{L_1} & 0 & 0 \\ \frac{1}{C_1} & \frac{-1}{RC_1} & 0 & \frac{-1}{RC_1} \\ 0 & 0 & 0 & 0 \\ 0 & \frac{-1}{RC_2} & 0 & \frac{-1}{RC_2} \end{bmatrix}, \quad B_2 = \begin{bmatrix} \frac{1}{L_1} \\ \frac{1}{RC_1} \\ \frac{1}{L_2} \\ \frac{1}{RC_2} \end{bmatrix} v_g \ . \tag{9}$$

By involving the duty cycle d, we can construct an average model as in (3) using (9). Then, equilibrium quantities can be obtained, which are denoted by $\overline{x}$ and $\overline{d}$. Then, using the steady-state condition $f(\overline{x}, \overline{d}) = 0$, we obtain

$$\overline{i}_{L_1} = \overline{i}_{L_2} = \frac{\overline{v}_{\text{out}}}{(1-\overline{d})R} \ ; \quad \overline{v}_{C_1} = \overline{v}_{C_2} = \frac{\overline{v}_g}{(1-\overline{d})}$$

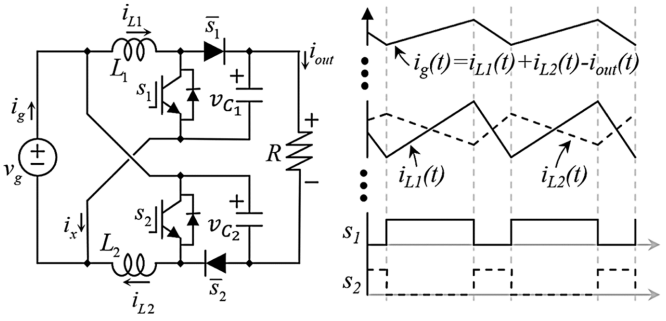

Fig. 3. Double dual boost converter topology with complementary duty cycles different than 0.5.

where $\overline{v}_{\text{out}} = \overline{v}_{C_1} + \overline{v}_{C_2} - \overline{v}_g$. This yields the input-to-output voltage gain

$$G := \frac{\overline{v}_{\text{out}}}{\overline{v}_g} = \frac{1-\overline{d}^2}{(1-\overline{d})^2} \, .$$

This converter exhibits a compelling high voltage gain and is able to cancel out the input current ripple. To do so, the switching signals of each transistor are 180° shifted with respect to each other, and their duty cycles are typically equal to 0.5. However, if a different gain is required, the use of complementary duty cycles is detrimental for the current ripple cancellation, as illustrated in Fig. 3.

In the following section, we discuss a method to overcome $\overline{d} = 0.5$ restriction. It is desired to select any voltage gain and simultaneously achieve perfect ripple cancellation and minimization over a region. The method is *implicit*, which means that it requires an inductor design procedure and a new modeling specification. Then, it can be implemented using a control strategy for voltage/current regulation.

IV. Implicit Current Ripple Cancellation Strategy

The topology used in this article is designed in such way that a minimum ripple input current can be achieved despite of moving the operation point. This technique considers equal slopes for the inductors but with opposite sign. As a result, a cancellation of the input current ripple is achieved.

Consider average modeling using (9), though this time using different duty cycles for each transistor, which are denoted by d_1 and d_2, whereas their steady-state value is expressed as $\overline{d}_1$ and $\overline{d}_2$. Define a duty cycle matrix $D := \left[\begin{smallmatrix} d_1 I_2 & 0_{2\times 2} \\ 0_{2\times 2} & d_2 I_2 \end{smallmatrix}\right]$. Then, compute

$$\frac{d}{dt}x = [DA_1 + (I_4 - D)A_2]\,x + DB_1 + (I_4 - D)B_2 \, . \quad (10)$$

Peak-to-peak current ripples of i_{L_1} and i_{L_2} are given by

$$i_{L_1(\text{ripple})} = \frac{\overline{v}_g}{L_1 f}\overline{d}_1 \, , \quad i_{L_2(\text{ripple})} = \frac{\overline{v}_g}{L_2 f}\overline{d}_2 \quad (11)$$

where f is the switching frequency. Note that the converter operates in CCM, as long as the dc component of the current through inductors is greater than or equal to half of the peak-to-peak current ripple, which can be expressed as

$$\frac{\overline{v}_{\text{out}}}{1-\overline{d}_j} \geq \frac{1}{2}\frac{\overline{v}_g \overline{d}_j}{L_j f}, \quad j = 1, 2 \, . \quad (12)$$

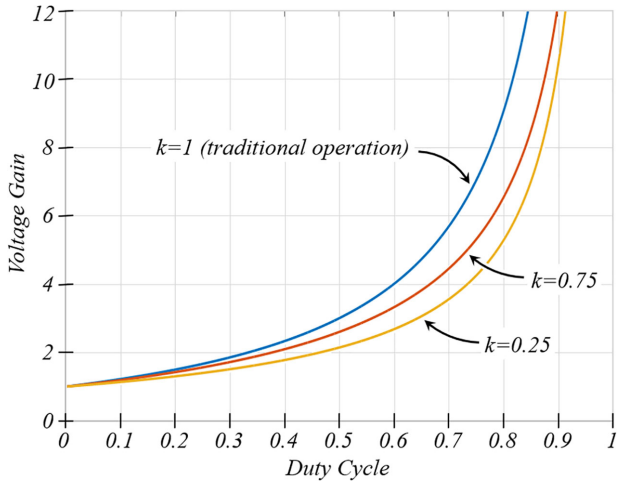

Fig. 4. Relation between the gain of the converter and the duty cycle for various values of k.

As long as the switching signal associated to each duty cycle has a carrier shifted 180° with respect to other, one converter exhibits a positive slope, whereas the other one is negative. Consequently, perfect ripple cancellation is in general achieved when $i_{L_1(\text{ripple})} = i_{L_2(\text{ripple})}$. According to (12), this is equivalent to

$$\frac{\overline{d}_1}{\overline{d}_2} = \frac{L_1}{L_2}.$$

Consequently, inductors can have different values by design, which are selected in such way that their ratio coincide with those of the duty cycles'. The latter can be expressed as

$$k := \frac{\overline{d}_1}{\overline{d}_2} \, . \quad (13)$$

Then, the condition of perfect cancellation can remain *implicit* in the design of the converter, as well as in its model. To do so, define $d := d_1 = kd_2$, for the duty cycles and $\overline{d} := \overline{d}_1 = k\overline{d}_2$ for their steady-state value. Notice that if $k = 1$, then duty cycles for the interleaved converter are the same, and the converter operates in the conventional operating point for interleaved converters, i.e., $\overline{d}_1 = \overline{d}_2 = 0.5$. On the other hand, if k is selected in such way that $L_1 \neq L_2$, then the operation point of the converter can be arbitrarily moved as well as the perfect ripple cancellation point. In this way, it is possible to achieve the freedom to select the gain of the converter, which is now given by

$$G := \frac{\overline{v}_{\text{out}}}{\overline{v}_g} = \frac{1-k\overline{d}^2}{1-\overline{d}(1+k)+k\overline{d}^2}. \quad (14)$$

In Fig. 4, we illustrate the voltage gain of the converter with respect to several values of duty cycle and the implicit inductance relation $k = L_1/L_2$.

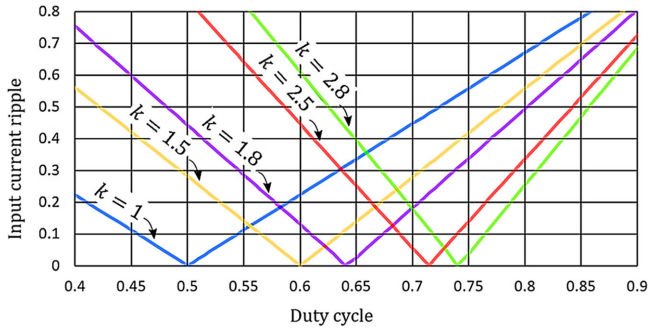

Fig. 5. Ripple against the value of the duty cycle for various values of k.

The advantage of this implicit approach is illustrated in Fig. 5. Note that the original constraint of a fixed duty cycle at 0.5 undermines the possibility to achieve higher voltage gains (using a higher duty cycle), without inducing a high input current ripple percentage. However, this point can be now arbitrarily moved with complete freedom to achieve high voltage gains and a minimal current ripple in a significantly wide neighborhood.

For design purposes, it can be of interest to have a formula to compute the nominal duty cycle $\overline{d}$, with respect to a desired voltage gain G. This is obtained from (14), i.e.,

$$\overline{d} = \frac{1 + \sqrt{1 - \frac{4}{1+G}}}{2}. \tag{15}$$

In Sections V and VI, the main contributions are introduced. In particular, two digital control strategies that operate along the implicit current ripple cancellation approach, described in this section, are introduced.

V. Discrete-Time Small-Signal Control Design

In this article, we use elements of *behavioral system theory* [26] to develop stability tests, as well as a discrete-time linear control technique for a double dual boost converter. We provide some preliminary background material of linear systems and Lyapunov stability in discrete time.

A. Linear Difference Systems

In general, a *linear difference system* can be expressed as

$$R_0 w + R_1(\sigma w) + \cdots + R_N(\sigma^N w) = 0 \tag{16}$$

where $w : \mathbb{N}_+ \to \mathbb{R}^q$ is a vector of discrete-time functions; N is the maximum degree of a shift operator σ; and $R_i \in \mathbb{R}^{p\times q}$, with $i = 0, 1, \ldots, N$. Equation (16) can be also represented as

$$R(\sigma)w = 0 \tag{17}$$

where $R(\sigma)$ is a polynomial matrix in σ. Stability properties of linear difference systems can be studied in terms of functionals called *quadratic difference forms* (QdFs) [27], which are functionals of w and its time shifts, i.e.,

$$Q_P(w) = \begin{bmatrix} w^\top & \sigma w^\top & \cdots & \sigma^N w^\top \end{bmatrix} P \begin{bmatrix} w \\ \sigma w \\ \vdots \\ \sigma^N w \end{bmatrix} \tag{18}$$

where P is called *coefficient matrix*. Analogous to the derivative operator in continuous time, the *rate of change* ∇Q_P of a functional Q_P is defined as $\nabla Q_P(w)(t) := \sigma Q_P(w)(t) - Q_P(w)(t)$.

Using QdFs, we can apply Lyapunov conditions to stability [28], which, in this article, are used to develop further algebraic specifications for stability and control design. For ease of reference, we recall these conditions.

A system represented by (16) is *asymptotically stable* if there exist Q_P such that for all w that satisfies (16), it holds

$$Q_P(w) \geq 0\,; \quad \nabla Q_P(w) < 0\,. \tag{19}$$

A QdF Q_P that satisfies the aforementioned inequalities is called *Lyapunov function*.

B. General Condition for Stability

A stability test using *linear matrix inequalities* (LMIs) can be obtained from conditions (19). To do so, note that such conditions are satisfied if there exists $Q_P \geq 0$ and polynomial matrices $V(\sigma)$ and $M(\sigma)$ of suitable sizes such that

$$\begin{aligned} \sigma Q_P(w) - Q_P(w) + w^\top R(\sigma)^\top V(\sigma) w + w^\top V(\sigma)^\top R(\sigma) w \\ = -w^\top M(\sigma)^\top M(\sigma) w. \end{aligned} \tag{20}$$

This can be accounted from the fact that for every w that satisfies $R(\sigma)w = 0$, it follows that

$$\underbrace{\sigma Q_P(w) - Q_P(w)}_{=:\nabla Q_K} = -\|M(\sigma)w\|_2^2 \tag{21}$$

which corresponds to a strictly negative rate of change, as required in (19).

C. Control Synthesis

In general, a linear feedback controller can adopt the following structure:

$$\sigma z = Az + Bu\,; \quad y = Cz + Du \tag{22}$$

where $z : \mathbb{N} \to \mathbb{R}^r$, $A \in \mathbb{R}^{r\times r}$, $B \in \mathbb{R}^{r\times n}$, $C \in \mathbb{R}^{1\times r}$, and $D \in \mathbb{R}^{1\times n}$. A state-feedback controller can be established by considering

$$y := \Delta d \text{ and } u := \Delta x\,. \tag{23}$$

The control design problem can be thus reformulated to finding matrices (A, B, C, D) such that the converter has an asymptotically stable equilibrium $(\overline{x}, \overline{d})$. To do so, consider (6), (22), and (23), that correspond to the closed-loop system. Then, the

following linear differential structure as in (17) can be obtained:

$$\underbrace{\begin{bmatrix} \sigma I_n - \overline{\mathbf{F}} & -\overline{\mathbf{G}} & 0_{n\times r} & 0_{n\times n} & 0_{n\times 1} \\ 0_{r\times n} & 0_{r\times 1} & \sigma I_r - A & -B & 0_{r\times 1} \\ 0_{1\times n} & 0_{1\times 1} & -C & -D & 1 \\ 0_{1\times n} & -1 & 0_{1\times r} & 0_{1\times n} & 1 \\ -I_n & 0_{n\times 1} & 0_{n\times r} & I_n & 0_{n\times 1} \end{bmatrix}}_{=:R(\sigma)} \underbrace{\begin{bmatrix} \Delta x \\ \Delta d \\ z \\ u \\ y \end{bmatrix}}_{=:w} = 0\,. \tag{24}$$

Note that the variables of interest in w include now the converter variables as well as those of the controller.

To develop an LMI equivalent to (21) that permit a numerical computation of the controller matrices (A, B, C, D), we factorize a matrix of coefficients $\widetilde{R}$ from (24) as

$$R(\sigma)w = \underbrace{\begin{bmatrix} R_0 & R_1 \end{bmatrix}}_{=:\widetilde{R}} \begin{bmatrix} w \\ \sigma w \end{bmatrix} \tag{25}$$

where

$$R_0 := \begin{bmatrix} -\overline{\mathbf{F}} & -\overline{\mathbf{G}} & 0_{n\times r} & 0_{n\times n} & 0_{n\times 1} \\ 0_{r\times n} & 0_{r\times 1} & -A & -B & 0_{r\times 1} \\ 0_{1\times n} & 0_{1\times 1} & -C & -D & 1 \\ 0_{1\times n} & -1 & 0_{1\times r} & 0_{1\times n} & 1 \\ -I_n & 0_{n\times 1} & 0_{n\times r} & I_n & 0_{n\times 1} \end{bmatrix}$$

$$R_1 := \begin{bmatrix} I_n & 0_{n\times 1} & 0_{n\times r} & 0_{n\times n} & 0_{n\times 1} \\ 0_{r\times n} & 0_{r\times 1} & I_r & 0_{r\times n} & 0_{r\times 1} \\ 0_{1\times n} & 0_{1\times 1} & 0_{1\times r} & 0_{1\times n} & 0 \\ 0_{1\times n} & 0 & 0_{1\times r} & 0_{1\times n} & 0 \\ 0_{n\times n} & 0_{n\times 1} & 0_{n\times r} & I_n & 0_{n\times 1} \end{bmatrix}.$$

Similarly, the coefficient matrix of $V(\sigma)$ in (21) can be congruently defined as $\widetilde{V} := \begin{bmatrix} V_0 & V_1 \end{bmatrix}$.

Then, using these coefficient matrices as well as the definition of a QdF in (18), (20) can be expressed as

$$\begin{bmatrix} w \\ \sigma w \end{bmatrix}^\top \begin{bmatrix} 0_{q\times q} & 0_{q\times q} \\ 0_{q\times q} & P \end{bmatrix} \begin{bmatrix} w \\ \sigma w \end{bmatrix} - \begin{bmatrix} w \\ \sigma w \end{bmatrix}^\top \begin{bmatrix} P & 0_{q\times q} \\ 0_{q\times q} & 0_{q\times q} \end{bmatrix} \begin{bmatrix} w \\ \sigma w \end{bmatrix} + \begin{bmatrix} w \\ \sigma w \end{bmatrix}^\top \widetilde{R}^\top \widetilde{V} \begin{bmatrix} w \\ \sigma w \end{bmatrix} + \begin{bmatrix} w \\ \sigma w \end{bmatrix}^\top \widetilde{V}^\top \widetilde{R} \begin{bmatrix} w \\ \sigma w \end{bmatrix} < 0 \tag{26}$$

where $P > 0$ has dimension $q \times q$, with $q := 2n + r + 2$; and the inequality "$<$" accounts for the negative element at the right-hand side of (20). Then, by standard linear algebra principles, the control synthesis problem is reduced to finding a matrix $P = P^\top > 0$ as well as the controller matrices (A, B, C, D) implicit in $\widetilde{R}$, and a matrix $\widetilde{V}$ that satisfy the following LMI:

$$\begin{bmatrix} 0_{q\times q} & 0_{q\times q} \\ 0_{q\times q} & P \end{bmatrix} - \begin{bmatrix} P & 0_{q\times q} \\ 0_{q\times q} & 0_{q\times q} \end{bmatrix} + \widetilde{R}^\top \widetilde{V} + \widetilde{V}^\top \widetilde{R} < 0. \tag{27}$$

Note that matrices P, $\widetilde{V}$ and the unknown elements in $\widetilde{R}$ can be numerically computed using standard LMI solvers, such as `Yalmip`.

Remark 1 (Robustness): The solution of (27) is robust with respect to the system and controller parameters. Consider (20). This equation has many solutions for different Lyapunov functions $Q_P(w)$ and polynomial matrices $M(\sigma)$. A polynomial approach to compute them is based on spectral factorization [29], i.e., by evaluation the aforementioned equation using $\sigma w^\top = -\lambda$ and $\sigma w = \lambda$, with $\lambda \in \mathbb{C}$, this yields

$$R(-\lambda)^\top V(\lambda) + V(-\lambda)^\top R(\lambda) = M(-\lambda)^\top M(\lambda)\,.$$

Here, we can identify the *maximal* Q_{P_+} and the *minimal* solution for Q_{P_-} that correspond to the Hurwitz and anti-Hurwitz spectral factors $M(\lambda)$, i.e., those with $\det(M(\lambda)) \neq 0$ with $\lambda < 1$ and $\lambda > 1$, respectively [29].

Then, *any* Lyapunov function Q_P satisfies $Q_{P_-} \leq Q_P \leq Q_{P_+}$. Moreover, a Lyapunov function Q_P can be computed as the convex combination of the extremes, i.e., $Q_P := aQ_{P_+} + (1-a)Q_{P_+}$ with $a \geq 0$. Due to (27). The family of solutions parameterized as a convex polytope also applies for the right-hand side of the equation, namely, the system and controller parameters. We conclude that the closed-loop system is a robust. ■

Remark 2(Generality as a Further Advantage): There are many LMI approaches to power converter control in the literature, see, e.g., [30], [31], which are based on a state-space setting (first-order difference/differential equations). In our case, we use a *linear difference approach* that also admits sets of higher order and zeroth-order equations as well. Moreover, the traditional Lyapunov-based LMI for state-space discrete time systems $A^\top PA - P < 0$ is a special case in this approach. To show this, compute the state-space realization of the interconnected system (24). To do so, compute a state map $X(\sigma)$ (see [32]), which induces a state vector $x = X(\sigma)w$. Compute $\sigma X(\sigma)$ modulo $R(\sigma)$, this means computing $\sigma X(\sigma)R(\sigma)^{-1} = P(\sigma) + S(\sigma)$, where $P(\sigma)$ is polynomial, whereas $S(\sigma)$ is strictly proper. Then, we obtain, for a square matrix A, the following equation $AX(\sigma)w = \sigma X(\sigma)w + B(\sigma)R(\sigma)w$, where $B(\sigma) := \lim_{\sigma\to\infty} \sigma X(\sigma)R(\sigma)^{-1}$. It can be easily verified that if $R(\sigma)$ contains only first-order elements, then $B(\sigma)$ is constant, denoted by B. This induces a classical autonomous state-space linear difference equation, now notice that substituting $(Ax)^\top PAx - x^\top Px < 0$ yields the following equation that can be compared with (20):

$$\underbrace{\sigma(x^\top Px) - x^\top Px}_{\sigma Q_P(w) - Q_P(w)} + \underbrace{w^\top R(\sigma)^\top B^\top Px}_{w^\top R(\sigma)^\top V(\sigma)w} + \underbrace{x^\top PBR(\sigma)w}_{w^\top V(\sigma)^\top R(\sigma)w} < 0\,.$$

In the state-space case $V(\sigma) = B^\top PX(\sigma)w$ and $Q_P(w) = w^\top X(\sigma)^\top PX(\sigma)w$. While in our case, $V(\sigma)$ has an arbitrary degree, which permits to include many other scenarios. The proposed approach is *modular*, i.e., it permits independent modeling of the plant and the controller with any structure and their interconnection is made via simple algebraic rules as in (22). This simplifies the analysis, which only requires to

directly add equations of arbitrary order without the need to construct a state-space model. ■

D. Application on the Double Dual Boost Converter

Note that this general specification in terms of matrices (A, B, C, D) admits any P, PI, PID, state- and output-feedback configuration. Nevertheless, although any computation of controller derived from (27) will guarantee stability, we might be interested in a particular structure that bring further desired specifications, such as time-response, disturbance rejection, controller order, etc.

In the case of the double dual boost converter, the corresponding small-signal discrete-time model can be obtained from (10), as specified in Section II-C, using the same incremental notation $\Delta x = x - \overline{x}$, and the implicit input current cancellation strategy $d := d_1 = kd_2$, then $\Delta x^\top := [\Delta i_{L_1} \quad \Delta v_{C_1} \quad \Delta i_{L_2} \quad \Delta v_{C_2}]^\top$ with respect to an average equilibrium

$$\overline{i}_{L_1} = \frac{\overline{v}_{\text{out}}}{(1-\overline{d})R} \; ; \; \overline{i}_{L_2} = \frac{\overline{v}_{\text{out}}}{(1-k\overline{d})R}$$

$$\overline{v}_{C_1} = \frac{\overline{v}_g}{1-\overline{d}} \; ; \; \overline{v}_{C_2} = \frac{\overline{v}_g}{1-k\overline{d}} \; .$$

The corresponding small-signal discrete-time model is thus computed as in (4), this yields

$$\overline{\mathbf{A}} := \begin{bmatrix} 0 & \frac{-(1-\overline{d})}{L_1} & 0 & 0 \\ \frac{(1-\overline{d})}{C_1} & \frac{-1}{RC_1} & 0 & \frac{-1}{RC_1} \\ 0 & 0 & 0 & \frac{-(1-k\overline{d})}{L_2} \\ 0 & \frac{-1}{RC_2} & \frac{1-k\overline{d}}{C_2} & \frac{-1}{RC_2} \end{bmatrix} \; , \; \overline{\mathbf{B}} := \begin{bmatrix} \frac{\overline{v}_{C_1}}{L_1} \\ \frac{-\overline{i}_{L_1}}{C_1} \\ \frac{\overline{v}_{C_2}}{L_2} \\ \frac{-\overline{i}_{L_2}}{C_2} \end{bmatrix} \; .$$

Then, we compute $\overline{\mathbf{F}} = e^{\overline{\mathbf{A}}h}$ and $\overline{\mathbf{G}} = \overline{\mathbf{A}}^{-1}(e^{\overline{\mathbf{A}}h} - I)\overline{\mathbf{B}}$.

In addition, the following controller structure is proposed:

$$\begin{cases} \Delta d = -k_1(\Delta i_{L_1} + \Delta i_{L_2} - r) \\ r = -k_2 z - k_3(\Delta v_{C_1} + \Delta v_{C_2}) \\ \sigma z = z + (\Delta v_{C_1} + \Delta v_{C_2}) \end{cases} \; . \tag{28}$$

Note that the controller in (28) can be accommodated in terms of the matrices (A, B, C, D) that are used in (25) and (27), i.e., $A := 1$, $B := [0 \quad 1 \quad 0 \quad 1]$, $C := k_2$, and $D := [-k_1 \quad k_3 \quad -k_1 \quad k_3]$.

Consequently, the value of gains $k_i, i = 1, 2, 3$, can be numerically computed by solving (27). The diagram of the controller is shown in Fig. 6, where k is the relation between inductors, as defined in (13).

VI. Discrete-Time Large-Signal Control Design

In this section, a (nonlinear) large-signal controller is introduced. The control design also considers the implicit current ripple cancellation strategy introduced in this article. The large-signal controller can be used in those cases where the converter is required to operate over a wide operation range, e.g., in trajectory tracking.

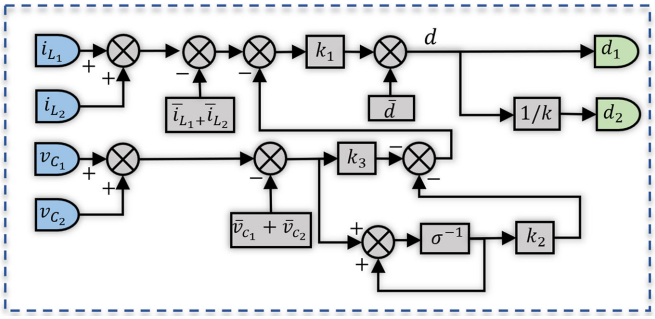

Fig. 6. Linear control loop comprising a current loop and a voltage loop.

A. Control Design

Consider the discrete-time large-signal model obtained from (10) in an analogous way as in Section II-D. Taking into account (9) and condition $d := d_1 = kd_2$, we can defined a matrix

$$K := \begin{bmatrix} I_2 & 0_{2\times 2} \\ 0_{2\times 2} & kI_2 \end{bmatrix}$$

and the matrices $A_{k,1} := KA_1$, $A_{k,2} := KA_2$, $B_{k,1} := KB_1$, and $B_{k,2} := KB_2$. Then, the following discrete-time large-signal model is obtained:

$$\begin{aligned} \sigma x = (I_n + A_{k,2}h)x + B_{k,2} \\ + \left[(A_{k,1} - A_{k,2})\, hx + (B_{k,1} - B_{k,2})\, h\right] d \; . \end{aligned} \tag{29}$$

We can transform the system into input–output coordinates by defining a *minimum-phase variable* (cf., [24]) denoted by y, i.e., $y = Hx$, with $H \in \mathbb{R}^{1\times n}$. Using (29), we compute

$$\begin{aligned} \sigma y = \sigma Hx = H(I_n + A_{k,2}h)x + HB_{k,2} \\ + H\left[(A_{k,1} - A_{k,2})\, hx + (B_{k,1} - B_{k,2})\, h\right] d \; . \end{aligned} \tag{30}$$

A general structure of the dynamics of a feedback controller is given by $\sigma z = \beta(x, z)$. Hence, define a *target system* that will determine the desired closed-loop performance of the converter as

$$\sigma \begin{bmatrix} y \\ z \end{bmatrix} = \begin{bmatrix} \phi(x, z) \\ \beta(x, z) \end{bmatrix} \; . \tag{31}$$

Then, by comparison of (30) and (31), solving for d, we obtain

$$d := \frac{\phi(y, z) - H(I_n + A_{k,2}h)x - HB_{k,2}}{H\left[(A_{k,1} - A_{k,2})\, hx + (B_{k,1} - B_{k,2})\, h\right]} \; . \tag{32}$$

Finally, although the freedom of choosing any pair of nonlinear vector spaces ϕ and β that satisfy these conditions is enabled, for easy of exposition and performance design, we can simply select

$$\phi(x, z) := -k_1(y - y^*); \quad \beta(x, z) := \begin{bmatrix} L & 1 \end{bmatrix} \begin{bmatrix} x \\ z \end{bmatrix} - r^* \tag{33}$$

with $y^* := -[k_2 \quad k_3 \, [\begin{smallmatrix} Lx \\ z \end{smallmatrix}]$, where $k_i > 0$, $i = 1, 2, 3$; Lx with $L \in \mathbb{R}^{1\times n}$ is the to-be-controlled variable and r^* is its desired reference trajectory.

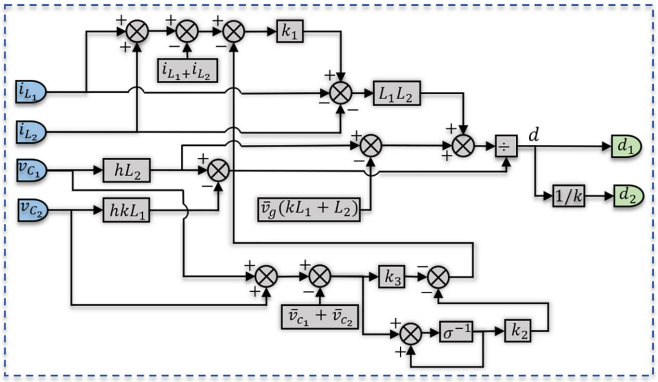

Fig. 7. Nonlinear controller comprising a current loop and an external voltage loop.

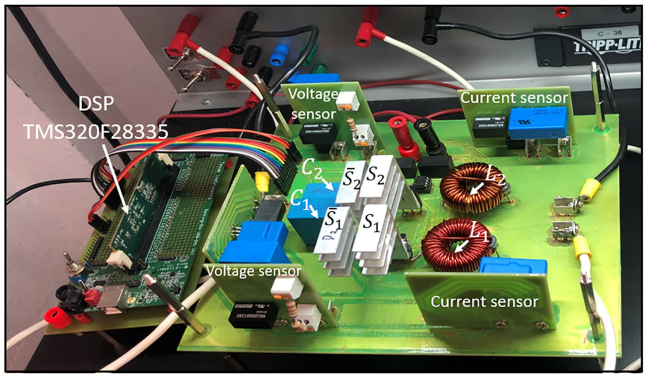

Fig. 8. Experimental prototype of double dual boost converter with DSP TMS320F28335. The implementation has the following nominal parameters: input voltage $v_g = 60$ V, output voltage $v_{\text{out}} = 210$ V, switching frequency 50 Khz, sampling time 10 μs, L_{1420} μH, $L_2 = 230$ μH, $C_1 = 8$ μF, $C_2 = 4.7$ μF, converter gain $G = 3.5$, and inductor relation $k = 1.8$.

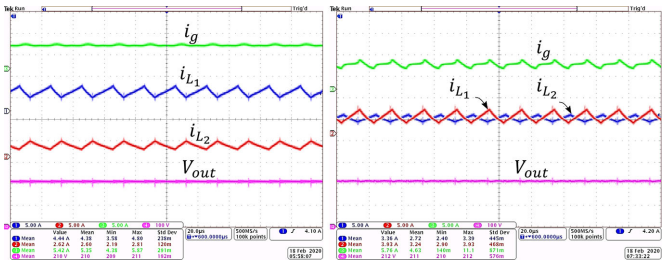

Fig. 9. Steady-state responses with $R = 140\,\Omega$ under: (a) the proposed input ripple cancellation strategy, and (b) a traditional current-balancing approach of: (from top to bottom) i_g (*y*-axis 5 A/div), i_{L1} (*y*-axis 5 A/div), i_{L2} (*y*-axis 5 A/div), V_{out} (*y*-axis 100 V/div) (in all cases, *x*-axis 20 μ s/div).

B. Stability Conditions

To guarantee global asymptotic stability, two steps are proposed. First, guaranteeing input-to-output stability, which involves stabilization of the minimum-phase variable. Internal stability is proved by the analysis of the *zero dynamics* (cf., [24]) of the closed-loop system.

1) Input-to-Output Stability: Consider the system $\sigma y = -k_1 y + k_1 y^*$. This system will be stable as long as y^* is bounded (internal stability of x and z) and $-k_1$ corresponds to a stable pole, i.e., $0 < k_1 < 1$ while estimating its best value in terms of, e.g., time response, can be given by the traditional relationship with the time constant τ, such that $k_1 = e^{-\frac{h}{\tau}}$ (see [17]).

2) Internal Stability: The zero dynamics of the system, i.e., $y(t_i) \equiv \overline{y}$ for all t_i, applied to the system (31) must guarantee $\lim_{t_i \to \infty} Lx(t_i) = r^*$. In the case of the double dual boost converter, it can be easily verified that internal stability is achieved by selecting $H = [1 \;\; 0 \;\; 1 \;\; 0$ and $L = [0 \;\; 1 \;\; 0 \;\; 1]$, which correspond to the selection of the sum of inductor currents as minimum phase variable and the output voltage as the to-be-controlled variable.

C. Application on the Double Dual Boost Converter

Consider the large-signal discrete-time model (29) constructed with matrices (9). The proposed nonlinear control design yields the duty cycle

$$d = \frac{(L_1L_2)(\phi(x,z) - i_1 - i_2) + hL_2v_{C_1} - (kL_1 + L_2)\overline{v}_g}{h(L_2v_{C_1} - kL_1v_{C_2})};$$

with $\phi(x,z)$ as in (33). The block diagram of the control loop is shown in Fig. 7.

VII. Experimental Results

In this section, experimental validation using a 300-W prototype is presented. An image of the experimental prototype is shown in Fig. 8. To show the advantages of the proposed controllers with the implicit current ripple cancellation technique, we also implement the traditional approach with constrained and complementary duty cycles (see e.g., [8], [13]–[16]). Moreover, we also change the operating region of the converter in both approaches to show the robustness as well as the current ripple cancellation capabilities of the controllers, which were implemented using a DSP TMS320F28335 with 100 kHz of sampling frequency. The gains for the controller in Fig. 6 are $k_1 = 0.001$, $k_2 = 0.0105$, and $k_3 = 0.0430$, whereas those of the controller of Fig. 7 are $k_1 = 0.1$, $k_2 = 0.081$, and $k_3 = 0.644$.

1) Small-Signal Current Ripple Cancellation Under Nominal Conditions With $R = 140\,\Omega$: In Fig. 9, the converter is tested under the nominal power with the load resistor $R = 140\,\Omega$ (i.e., $P = 315$ W). Fig. 9(a) depicts the proposed (small-signal) closed-loop voltage regulation and input-current cancellation technique. Fig. 9(b) shows the traditional approach without the proposed implicit current-cancellation technique and complementary duty cycles. Note that under the traditional current approach, the input current exhibits a considerable current ripple i_g, whereas under the proposed ripple cancellation technique, the ripple is practically cancelled.

2) Small-Signal Current Ripple Cancellation With $R = 100\,\Omega$: A similar result is obtained with the converter operating at different point than the nominal, we use $R = 100\,\Omega$, i.e., 440 W, this is shown in Fig. 10. Fig. 10(a) depicts the

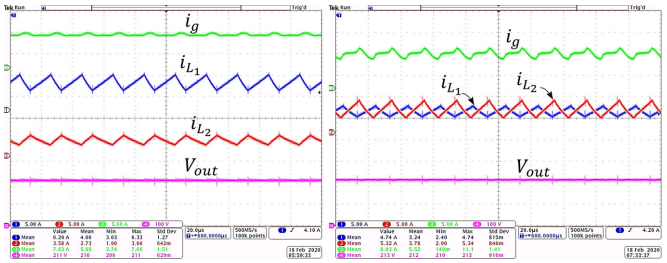

Fig. 10. Steady-state responses with $R = 100\,\Omega$ under: (a) the proposed input ripple cancellation strategy, and (b) a traditional current-balancing approach of: (from top to bottom) i_g (y -axis 5 A/div), i_{L1} (y -axis 5 A/div), i_{L2} (y -axis 5 A/div), V_{out} (y -axis 100 V/div) (in all cases, x -axis 20 μs/div).

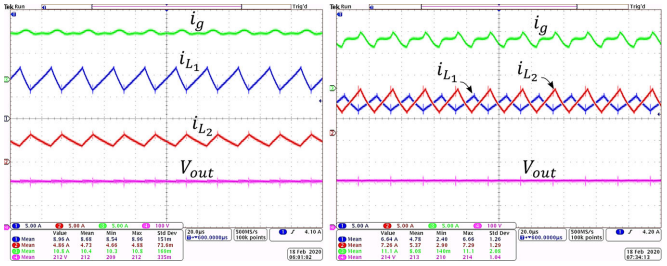

Fig. 11. Steady-state responses with $R = 74\,\Omega$ under: (a) the proposed input ripple cancellation strategy, and (b) a traditional current-balancing approach of: (from top to bottom) i_g (y -axis 5 A/div), i_{L1} (y -axis 5 A/div), i_{L2} (y -axis 5 A/div), V_{out} (y -axis 100 V/div) (in all cases, x -axis 20 μs/div).

proposed (small-signal) closed-loop voltage regulation and input-current cancellation technique. Fig. 10(b) shows the traditional approach. Note that under the traditional approach, the converter operates with a considerable input current ripple i_g, whereas the proposed technique maintains good cancellation despite of the fact that the converter is operating significantly above its nominal power specification.

3) Small-Signal Current Ripple Cancellation With $R = 74\,\Omega$***:*** The controller was also tested at twice the nominal power (i.e., $P = 600\,\text{W}$), using $R = 74\,\Omega$; the results are shown in Fig. 11. Note that in the previous cases, and although the converter and the controller are operating in an extreme operating point of twice the nominal design, the proposed technique exhibits a good ripple cancellation profile on i_g while the traditional approach exhibits poor cancellation.

4) Large-Signal Current Ripple Cancellation With $R = 74\,\Omega$***:*** The nonlinear controller was also tested at the same points of operation, the result at the input current ripple i_g is very similar to the liner case. In Fig. 12, the converter operates with $R = 140\,\Omega$, which is its nominal value. In Fig. 13, the converter operates at 430 W under a load of $R = 100\,\Omega$. Finally, the converter at twice the nominal power (i.e., $P = 600\,\text{W}$), with $R = 74\,\Omega$ is shown in Fig. 14. Note that the large-signal controller exhibits current ripple cancellation capabilities, as suitable as its small-signal counterpart. This is possible even under extreme variations on its nominal operation. Steady-state operation and current ripple cancellation are in completely agreement with the small-signal counterpart. Experiments are

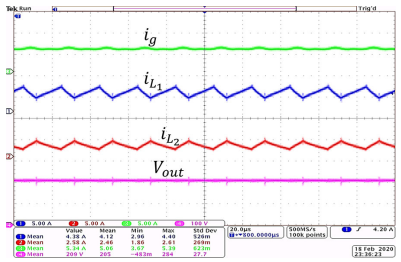

Fig. 12. Steady-state response under the nonlinear controller at a load of $R = 140\,\Omega$ of: (from top to bottom) i_g (y -axis 5 A/div), i_{L1} (y -axis 5 A/div), i_{L2} (y -axis 5 A/div), and V_{out} (y -axis 100 V/div) (in all cases, x -axis 20 μs/div).

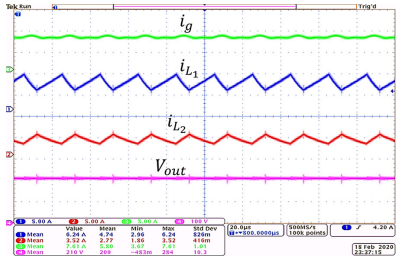

Fig. 13. Steady-state response under the nonlinear controller at a load of $R = 100\,\Omega$ of: (from top to bottom) i_g (y -axis 5 A/div), i_{L1} (y -axis 5 A/div), i_{L2} (y -axis 5 A/div), and V_{out} (y -axis 100 V/div) (in all cases, x -axis 20 μs/div).

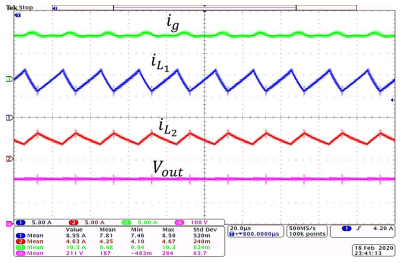

Fig. 14. Steady-state response under the nonlinear controller at a load of $R = 74\,\Omega$ of: (from top to bottom) i_g (y -axis 5 A/div), i_{L1} (y -axis 5 A/div), i_{L2} (y -axis 5 A/div), and V_{out} (y -axis 100 V/div) (in all cases, x -axis 20 μs/div).

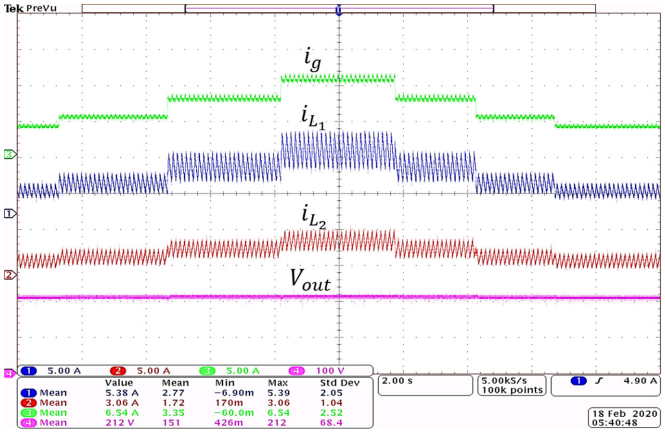

Fig. 15. Transient responses under the linear control against stepwise load changes from 200 to 150 Ω, to 100 Ω, to 75 Ω, to 100 Ω, to 150 Ω and, finally, to 200 Ω with a set-point of $V_{\text{out}} = 210$ V of: (from top to bottom) i_g (y -axis 5 A/div), i_{L1} (y -axis 5 A/div), i_{L2} (y -axis 5 A/div), and V_{out} (y -axis 100 V/div) (in all cases, x -axis 2 s/div).

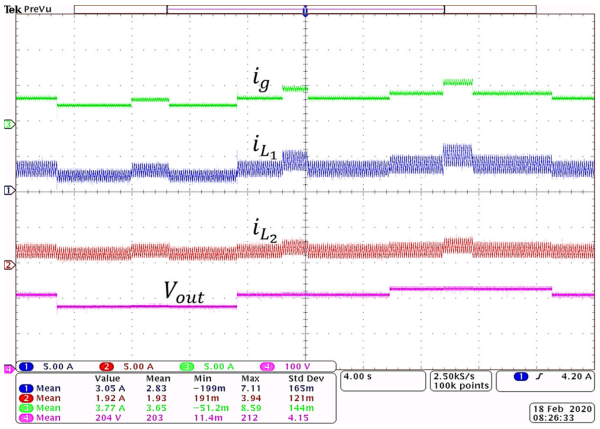

Fig. 16. Transient responses under the nonlinear control against stepwise load changes from 200 to 150 Ω, to 200 Ω in each voltage reference with changes in the voltage reference from $V_{\text{out}} = 210$ V to $V_{\text{out}} = 170$ V, to $V_{\text{out}} = 210$ V, to $V_{\text{out}} = 230$ V and, finally, to $V_{\text{out}} = 210$ V of: (from top to bottom) i_g (y-axis 5 A/div), i_{L1} (y-axis 5 A/div), i_{L2} (y-axis 5 A/div), and V_{out} (y-axis 100 V/div) (in all cases, x-axis 2 s/div).

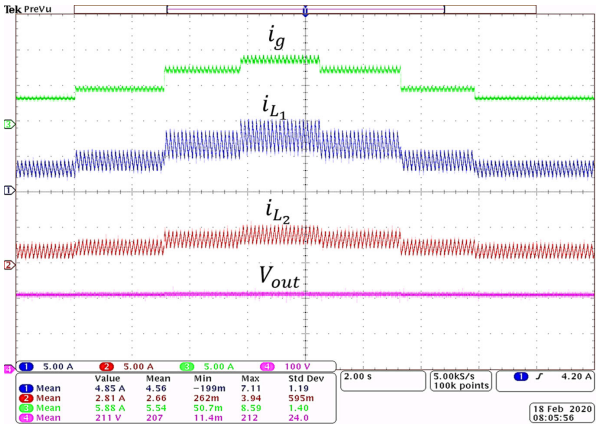

Fig. 17. Transient responses under the nonlinear control against stepwise load changes from 200 to 150 Ω, to 100 Ω, to 75 Ω, to 100 Ω, to 150 Ω and, finally, to 200 Ω with a set-point of $V_{\text{out}} = 210$ V of: (from top to bottom) i_g (y-axis 5 A/div), i_{L1} (y-axis 5 A/div), i_{L2} (y-axis 5 A/div), and V_{out} (y-axis 100 V/div) (in all cases, x-axis 2 s/div).

anyway included to illustrate the capabilities of both controllers to operate over a wide operating region.

5) Small- and Large-Signal Controller Dynamic Responses With Respect to Abrupt Control Reference and Load Variations: In Fig. 16, the controller was tested under changes in the voltage reference, whereas in each new voltage reference, load changes were applied, voltage steps of ±10% were applied together with load changes between 200 and 150 Ω. Note that the output voltage remains at its reference value even when load changes are applied. In Fig. 15 and Fig. 17, the response of the linear and nonlinear controller was tested under different loads, moving stepwise adopting several values between 200 and 75 Ω. Note that despite of load changes, which induces different operating region, far away from the design point, the input current ripple remains always small. The same voltage reference steps were applied to the nonlinear controller, voltage steps of ±10% were applied together with load changes between 200 and 150 Ω. Similarly, in Fig. 18, we show the nonlinear controller response under the similar steps changes. The output voltage remains practically constant while the input current ripple maintains a minimum value.

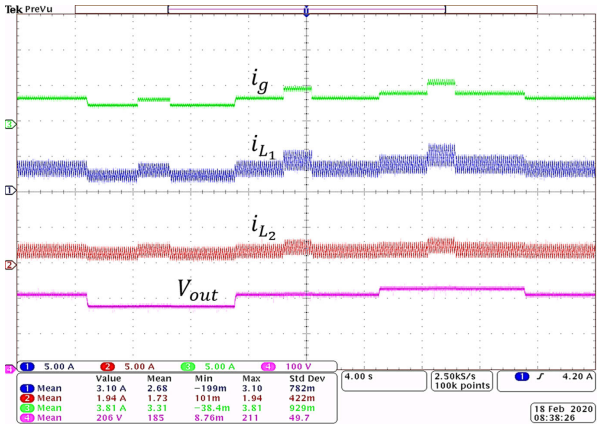

Fig. 18. Transient responses under the nonlinear control against stepwise load changes from 200 to 150 Ω to 200 Ω in each voltage reference with changes in the voltage reference from $V_{\text{out}} = 210$ V, to $V_{\text{out}} = 170$ V, to $V_{\text{out}} = 210$ V, to $V_{\text{out}} = 230$ V and, finally, to $V_{\text{out}} = 210$ V of: (from top to bottom) i_g (y-axis 5 A/div), i_{L1} (y-axis 5 A/div), i_{L2} (y-axis 5 A/div), and V_{out} (y-axis 100 V/div) (in all cases, x-axis 2 s/div).

VIII. Conclusion

The main contributions found in this article were as follows. An implicit current ripple cancellation technique was introduced and we showed that an unconstrained selection of the converter operating region can be achieved, without affecting the current ripple cancellation property. New small-signal and large-signal discrete-time models were introduced. These models guaranteed current ripple cancellation when combined with current/voltage controllers. A novel linear difference system approach was introduced. This setting permits to incorporate discrete-time converter models and controllers in a modular way, admitting high-order as well as zeroth-order equations in the closed-loop modeling. New stability conditions in terms of LMIs were proposed. These were based on Lyapunov stability theory for QdFs and were used for gain tuning purposes. The proposed controllers were able to work over a wide operating region. The linear controller was robust with respect to nominal parameter specifications, whereas the nonlinear controller worked intrinsically over a large-signal domain. The current ripple was minimized even over significantly parameter, power, and set-point variations. The ripple cancellation technique implicit in the controllers also holds under extreme circumstances, as illustrated in the experimental results.

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Chapter 4

A Double Dual Boost Converter with Switching Ripple Cancellation for PEMFC Systems

Summary of the chapter

This chapter presents an article in which a current-based control for a proton-exchange membrane fuel cell using the so-called double dual boost topology is studied. In particular, we introduce a discrete time controller that, in coordination with a particular selection of inductors and capacitors, minimizes the switching ripple at the input port (current ripple) and the output port (voltage ripple) of the double dual boost converter. This converter has a particular characteristic, in contrast to the classical interleaved boost topology, in the double dual boost, the phases of the converter can have different duty ratios. The freedom to choose the duty ration for each phase can be used to select the operative point in which the input current is equal to zero. However, if individual controllers are used for each branch of the converter, the equilibrium after a transient can differ from the minimum ripple operation point; the proposed scheme regulates the output voltage and, at the same time, ensures the equilibrium remains in the minimum ripple operation in steady state. In this way, the converter can mitigate the harmonic distortion on the current extracted from the proton-exchange membrane fuel cell, which is beneficial to improve the effciency and lifetime of the cell, and on the output voltage delivered to an output direct current bus. The results of the experiment are presented to validate the principles of the proposed system.

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A Double Dual Boost Converter with Switching Ripple Cancellation for PEMFC Systems

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Abstract: This paper presents a current-based control for a proton-exchange membrane fuel cell using the so-called double dual boost topology. In particular, we introduce a discrete time controller that, in coordination with a particular selection of inductors and capacitors, minimizes the switching ripple at the input port (current ripple) and the output port (voltage ripple) of the double dual boost converter. This converter has a particular characteristic, in contrast to the classical interleaved boost topology, in the double dual boost, the phases of the converter can have different duty ratios. The freedom to choose the duty ration for each phase can be used to select the operative point in which the input current is equal to zero. However, if individual controllers are used for each branch of the converter, the equilibrium after a transient can differ from the minimum ripple operation point; the proposed scheme regulates the output voltage and, at the same time, ensures the equilibrium remains in the minimum ripple operation in steady state. In this way, the converter can mitigate the harmonic distortion on the current extracted from the proton-exchange membrane fuel cell, which is beneficial to improve the efficiency and lifetime of the cell, and on the output voltage delivered to an output direct current bus. The results of the experiment are presented to validate the principles of the proposed system.

Keywords: DC–DC converters; power electronics; PWM converters; current ripple cancellation

1. Introduction

Fuel cells (FCs) and other renewable energy sources are a compelling alternative to conventional pollution-prone power sources [1–4]. However, there are additional relevant challenges that must be solved to propagate them. For instance, the requirement of voltage or current regulation under wide ranges of operating conditions using power converters. Another important challenge is related to the low amplitude of the output voltage; the output voltage of the fuel cell must be increased and regulated to feed a grid-tie inverter. For instance, the voltage of a traditional fuel cell (FC) stack can be in the order of dozens of volts, while the DC bus voltage requirements for a grid tie inverter are several times higher [1,2]. Furthermore, the input current of some power converters can be a discontinuous signal or a continuous signal with a large switching ripple (variations due to the switching action). This current is drawn from the fuel cell, with a negative impact on the lifetime and performance of fuel

cells, as mentioned in several investigations [1,2]. The negative effect of distorted current signals on fuel cells has motivated new investigations [5–9]. It is recommended that the FC current ripple must be lower than 5% to have a good performance. In order to overcome this challenge, new topologies have been designed to operate with lower current ripples than traditional topologies and to provide high voltage gains [3,4].

Several converter topologies can overcome the discussed challenges; for example, quadratic-gain converters ([10,11]) achieve a large voltage gain. The large voltage gain can be used to increase the voltage provided by the fuel cell; the main disadvantage of quadratic converters is the voltage stress across their transistor; this produces a relatively large amount of switching power losses.

Another solution to provide a large voltage gain are multilevel topologies [12,13], which have lower voltage-stress on transistors; on the other hand, multilevel converters contain a significant number of semiconductor devices.

Switched inductor topologies [14,15] and coupled inductors [16,17] have been are also used. Another solution involves switched-capacitor topologies [18,19], which overcome some of those challenges; they feature small size/weight and high power density; however, their best performance and efficiency are obtained in cases in which there is no voltage regulation.

A topology option with large voltage gain and switching ripple cancellation is the one introduced in [20], where it was called the double dual boost converter (DDBC) [20–23]. In general, it has been shown that the DDBC can achieve input current ripple cancellation and overall satisfactory performance in experimental implementations [20–23].

This article presents the implementation of a fuel cell generation system. The base of the generation system is a dc–dc converter of a topology called double dual boost converter. The system implementation includes the design of the converter and its experimental validation. The system also includes a closed-loop digital controller. The controller, in coordination with a particular selection of inductors and capacitors, minimizes the switching ripple on the topology, both switching ripples, the input current ripple, and the output voltage ripple. The work includes a hardware-in-the-loop closed-loop implementation, rather than passive based with respect to a fixed operating point, as in the current literature.

This article describes a fully integrated solution to the described challenges. It comprises the hardware in the loop interconnection of two independently controlled systems (the fuel cell emulator and the double dual boost converter). The obtained experimental results involve the design and validation of an FC emulator and a correct selection of passive components (capacitors and inductors) for the converter, along with the controller design in discrete time, which ensures the active minimization of switching ripples. Experimental results are provided to validate the principle of the proposition.

2. Methodology

This article is focused on the dc–dc converter, with particular hardware design and a particular digital controller; the converter is suitable for their use in a fuel-cell based generation system; in order to corroborate their operation, this work started with the design and implementation of a fuel cell emulator based on the hardware in the loop philosophy.

Figure 1 shows the fuel cell emulator, which is based on a controlled dc source, an FPGA-compact Rio 9039 (from National Instruments, Austin, TX, USA) data acquisition system, and a computer with LabView software; the computer program is based on a fuel cell mathematical model which is described on Section 6 of this article. The emulator was built and validated before their connection to the dc–dc double dual boost converter. The power controlled source used for the fuel cell emulator was the Keysight N6953A model (from Keysight Technologies, Santa Rosa, CA, USA).

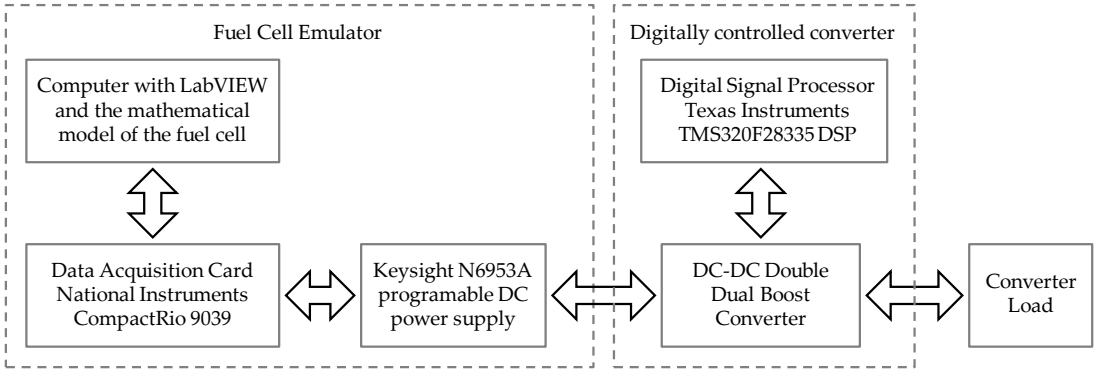

Figure 1. The full hardware in the loop system developed for this article.

The output of the fuel cell emulator is connected to the double dual boost converter; this particular topology of the converter is described in Section 3 of this article; the experiment was designed in order to validate the implementation of the proposed discrete-time controller under a realistic scenario.

The particular hardware design of the converter is discussed in Section 4 of this article, and the digital control loop is described in Section 5 of this article. The digital controller was implemented on a Texas Instruments TMS320F28335 digital signal processor (From Texas Instruments, Dallas, TX, UAS), see Figure 1.

After the fuel cell emulator was build and tested (some experiments in the experimental results demonstrate their operation), the DDBC was designed, implemented, and tested in open-loop mode. Once the converter operates properly in open-loop mode, a digital controller was designed and tested. To control the converter, the Texas Instruments TMS320F28335 digital signal controller was used.

Finally, the complete system was integrated, and proper operation test was carried out; the two independently controlled systems operated correctly, as shown in the experimental results section, which is Section 7 of this article.

3. The Double Dual Boost Converter (DDBC)

We briefly discuss the main features of the DDBC [20–23], which is depicted in Figure 2. The DDBC is based on two boost sub-circuits that are connected in input parallel and output series. The difference of this section with most descriptions of the converter in the state of the art is that we are not assuming that both sub-circuits have the same duty; they actually have different duty cycles. The sub-circuit that contains L_1, C_1, S_1, and $\bar{S}_1$, is called the upper switching stage, while the lower switching stage contains L_2, C_2, S_2, and $\bar{S}_2$.

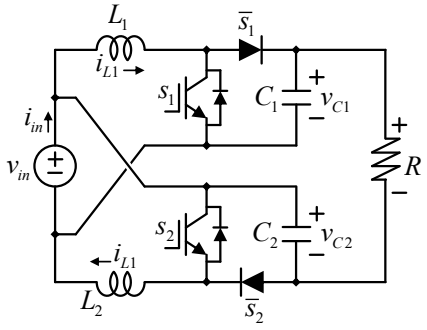

Figure 2. The topology of a double dual boost converter (DDBC).

For ease of exposition, the converter is assumed to operate in continuous conduction mode. Consequently, when the upper diode is closed, then the upper transistor is open and vice versa; the same consideration applies to the lower switching stage.

The converter operates with the Pulse Width Modulation PWM, which can be explained in the following manner: a defined and constant switching frequency for transistors. The inverse of the switching frequency is the switching period. A duty ratio or duty cycle is the relation among the time a transistor is closed, divided over the total switching period. Figure 3a shows the relevant waveforms when operating with a duty cycle $D = 0.7$.

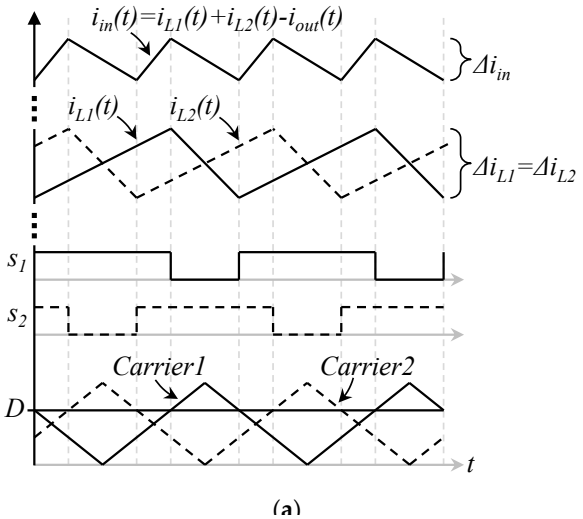

Figure 3. Relevant waveforms in the DDBC (**a**) with a duty ratio of 70%, (**b**) with a duty ratio of 30%.

Figure 3b shows the same waveforms as Figure 3a, but in this case, the duty ratio $D = 0.3$. The signals s_1 and s_2 are digital functions, which means they have only two values, 0 or 1, high or low. They are called switching functions because they define the operation of transistors (remember that a transistor is closed, or turned on, when the transistor is open). Switching functions are obtained from the comparison of two triangular carriers (Carrier1 and Carrier2), shifted 180° with duty cycle. The duty cycle seems such a constant value in Figure 3. The relation among the on-time and the switching period can be observed from switching functions, and it can also be expressed as the relation among the constant signal D, divided over the peak value of the triangular carriers.

period can be observed from switching functions, and it can also be expressed as the relation among the constant signal D, divided over the peak value of the triangular carriers.

Both inductors have the same inductance, and the same duty cycle is used for both switching stages. Note that the input current is equal to the sum of the current through both inductors minus the output current. The input current ripple is thus smaller to the sum of inductor currents. In former studies ([20–23]), transistors are driven by the same duty cycle. However, the converter sub-circuits can have different switching functions without restrictions on the duty cycle.

The input-to-output voltage gain of the DDBC converter is now computed. We use the notation D_1 to refer to the duty cycle of the upper switching stage, and D_2 is used for that of the lower one. This time there is no restriction for D_1 to be equal to D_2. The mathematical model of the converter can be obtained with the traditional averaging technique and described as Equations (1)–(4).

$$L_1 \frac{di_{L1}}{dt} = d_1 v_{in} + (1 - d_1)(v_{in} - v_{C1}) \tag{1}$$

$$C_1 \frac{dv_{C1}}{dt} = (1 - d_1) i_{L1} - i_{out} \tag{2}$$

$$L_2 \frac{di_{L2}}{dt} = d_2 v_{in} + (1 - d_2)(v_{in} - v_{C2}) \tag{3}$$

$$C_2 \frac{dv_{C2}}{dt} = (1 - d_2) i_{L2} - i_{out} \tag{4}$$

On Equations (1)–(4) as well as in Figure 2, v_{in} is the input voltage, L_1 and L_2, inductors 1 and 2 respectively, C_1 and C_2 capacitors 1 and 2 respectively, d_1 and d_2 duty cycles for transistors s_1 and s_2 respectively, i_{L1} and i_{L2} are the currents through inductors L_1 and L_2, and v_{C1} and v_{C2} are the voltages across the capacitors C_1 and C_2. Finally, i_{out} is the output current of the converter.

Another important equation, which is related to the input current ripple cancelation that will be further explained, is the definition of the input current in terms of the summation of the current through inductors and the output current.

$$i_{in} = i_{L1} + i_{L2} - i_{out} \tag{5}$$

In steady state, considering that voltage in capacitors and current through inductors comply with the small ripple approximation, the average voltage across the inductors. This yields to

$$V_{out} = V_{C1} + V_{C2} - V_{in} = \frac{V_{in}}{1 - D_1} + \frac{V_{in}}{1 - D_2} - V_{in} = V_{in} \frac{1 - D_1 D_2}{1 - D_1 - D_2 + D_1 D_2} \tag{6}$$

$$I_{Lj} = \frac{I_{out}}{1 - D d_j} = \frac{V_{out}}{\left(1 - D_j\right) R} \tag{7}$$

The difference from upper case to lower case in all variables, for instead from d_1 to D_1, indicates the operation regime. The upper case shows the steady-state value, which means no transient or perturbation is present, while the lower case shows the large-signal value, which includes transient behaviors. That is the reason why Equations (1) to (4) are all in lower case, while (6) and (7) are upper case. For example, V_{C1} represents the steady-state component of v_{C1}.

As a special case in this approach, which leads to the traditional approach, if $D_1 = D_2 = D$ in (6), then the well-known gain of the double dual boost converter is obtained.

The voltage rating in transistors (the voltage transistors block when they are open) can be expressed as (8).

$$V_{s1} = \frac{V_{in}}{1 - D_1};\ V_{s2} = \frac{V_{in}}{1 - D_2} \tag{8}$$

4. Input Current and Output Voltage Ripple Minimization

Though perfect cancellation of input–current–ripple is a desired characteristic in interleaved converters; it is well-known that this condition is only achievable at specific gains in traditional designs [20–23]. In contrast with traditional approaches, as mentioned before, in the DDBC, the desired duty cycle can be arbitrarily selected according to the nominal voltage gain, e.g., the case when the duty cycles are linearly dependent; this issue is elaborated in the following: Define D as the base duty cycle for the converter, i.e., $D = D_1$; both D_1 and D_2, can be expressed as a function of the duty cycle D, as shown in Equation (9).

$$D_1 = D;\ D_2 = kD \tag{9}$$

Duty ratios D_1 and D_2 take values between 0 and 1, at any time. Equation (6) can be written as Equation (10) after substituting Equation (9).

$$G = \frac{V_{out}}{V_{in}} = \frac{1}{1-D} + \frac{1}{1-kD} - 1 \tag{10}$$

Being G, the topology voltage gain and k is the constant factor that relates the duty cycle D of the converter to the individual duty cycle of each phase D_1 and D_2. Equation (10) can be written as Equation (11) after substituting Equation (9):

$$G = \frac{V_{out}}{V_{in}} = \frac{1-kD^2}{1-D(1+k)+kD^2} \tag{11}$$

In order to achieve a total ripple cancellation, there are two conditions that must be satisfied: (i) the current positive derivative of one inductor should be equal to the current negative derivative of the other inductor and vice versa; (ii) the total current ripple of both inductors must have equal magnitude shifted 180°. The second condition can be expressed as:

$$\Delta_{iL1} = \frac{V_g}{L_1} D_1 T_s = \Delta_{iL2} = \frac{V_g}{L_2} D_2 T_s \tag{12}$$

where Δi_{L1} and Δi_{L2} are the inductor current ripples, and T_S is the switching period of the converter. Using (12) and (9), we can conclude that $L_2 = kL_1$. Considering that D_1 and D_2 are complementary for an operating condition with complete cancellation, this yields:

$$\frac{V_g}{L_1} D^* T_s = \frac{V_g}{kL_1} (1-D^*) T_s \Rightarrow k = \frac{1-D^*}{D^*} \tag{13}$$

Note that D^* represents the nominal duty cycle at which the current ripple is completely mitigated. D^* is constant, D can adopt a value among 0 and 1. The duty ratio in (10) is obtained from (13), for a certain gain G as:

$$D^* = \frac{1 + \sqrt{1 - \frac{4}{1+G}}}{2} \tag{14}$$

Note that (14) has two solutions. The one associated with a minus before the square root would lead to a different k and D^*. If this value is used, the same result is obtained in terms of current ripple cancellation, but the role of the switching stages would be inverted. The designer must consider the power distribution among the different phases of the converter; the designer selects the power rate of the components during the design state. For simplicity, we will follow only one root of (14). Note that k has a minor impact on the gain, which mainly depends on D.

The output voltage switching ripple cancellation is the other crucial characteristic of the converter. Similar to the current ripple cancellation, the current I_{out} charges the capacitor C_1 during the time DT_S, and at the same time, the capacitor C_2 is being charged with the current equal to $I_{L2} - I_{out}$. Moreover,

during the period of time $(1 - D)T_S$, capacitor C_2 is discharged by means I_{out}, and C_2 is discharged due to a current equal to $I_{L2} - I_{out}$. To accomplish the output voltage ripple cancellation, we can establish two conditions. (i) The positive voltage derivative in one capacitor must coincide with the negative voltage derivative in the other, and vice versa; (ii) The total voltage ripple of both capacitors must have the same magnitude. The first is satisfied when $D = D^*$. For the second condition, by considering the voltage ripple equation, we have:

$$\Delta v_{C1} = \frac{I_{out}}{C_1} D^* T_s = \Delta v_{C2} = \frac{I_{out}}{C_2}(1 - D^*)T_s \tag{15}$$

From (15), we can conclude that the relationship between C_1 and C_2 is given by

$$\frac{C_1}{C_2} = \frac{D^*}{1 - D^*} = \frac{1}{k} \tag{16}$$

Then, in order to achieve the simultaneous output voltage ripple and input current ripple cancelation, capacitors must be selected in a way that $C_2 = kC_1$, as well as in inductors.

5. Digital Control of the Converter with Switching Ripple Cancelation

This section focusses on the dynamical behavior and the switching ripple cancelation to design a closed-loop controller with the desired characteristics. The dynamic model of the converter is described by (17). The model (17) considers Equations (1) and (2) as well as the constant k that is determined by design using (13) and (16).

$$\begin{cases} L_1 \frac{di_{L1}}{dt} = v_{in} - (1-d)v_{C1} \\ L_2 \frac{di_{L2}}{dt} = v_{in} - (1-kd)v_{C2} \\ C_1 \frac{dv_{C1}}{dt} = (1-d)i_{L1} - \frac{v_{C1}+v_{C2}-v_{in}}{R} \\ C_2 \frac{dv_{C2}}{dt} = (1-d)i_{L2} - \frac{v_{C1}+v_{C2}-v_{in}}{R} \end{cases} \tag{17}$$

where v_{C1}, v_{C2}, i_{L1}, i_{L2} are the state variables, v_{in} is a non-controller input of the system, which is also a variable, and d is the control input of the system, the variable that we can change to control the output voltage.

From (17), the small-signal linearization technique can be applied to get the small-signal model, which is expressed as:

$$\frac{d}{dt}\begin{bmatrix} \delta i_{L1} \\ \delta i_{L2} \\ \delta v_{C1} \\ \delta v_{C2} \end{bmatrix} = \begin{bmatrix} 0 & \frac{(1-\overline{D})}{L_1} & 0 & 0 \\ 0 & 0 & 0 & -\frac{(1-k\overline{D})}{L_2} \\ \frac{(1-\overline{D})}{C_1} & -\frac{1}{RC_1} & 0 & -\frac{1}{RC_1} \\ 0 & -\frac{1}{RC_2} & \frac{(1-k\overline{D})}{C_2} & -\frac{1}{RC_2} \end{bmatrix} \begin{bmatrix} \delta i_{L1} \\ \delta i_{L2} \\ \delta v_{C1} \\ \delta v_{C2} \end{bmatrix} + \begin{bmatrix} \frac{\overline{V}_{C1}}{L_1} \\ \frac{k\overline{V}_{C2}}{L_2} \\ \frac{-\overline{I}_{L1}}{C_1} \\ \frac{-k\overline{I}_{L2}}{C_2} \end{bmatrix} \delta D \tag{18}$$

This model in (18) is expressed in incremental variables, where $\delta I_j = I_{L1} - \overline{I}_{L1}$ is the increment of I_{L1} in reference to the equilibrium reference value I_{L1}, and so on for the other variables. In the following, we consider the discrete-time version of (18), which can be obtained by standard methods. Then, we obtain a state-space linear difference system of the form

$$\begin{bmatrix} \delta i_{L1}(n+1) \\ \delta i_{L2}(n+1) \\ \delta v_{C1}(n+1) \\ \delta v_{C2}(n+1) \end{bmatrix} = A \begin{bmatrix} \delta i_{L1}(n) \\ \delta i_{L2}(n) \\ \delta v_{C1}(n) \\ \delta v_{C2}(n) \end{bmatrix} + B\delta D(n) \tag{19}$$

where n represents the time; and A and B are constant matrices of dimension 4×4 and 4×1, respectively.

We aim at guaranteeing the regulation of input current. Hence, a current control-loop is realized with the controller in Equation (20).

$$\delta D(n) := -k_1 x(n) - k_2(\delta i_{L1}(n) + \delta i_{L2}(n)) \tag{20}$$

where k_1, k_2 are the controller gains; x_1, is the error-integral of $(\delta i_1(n) + \delta i_2(n))$ in which the state-space expression is (21).

$$x(n+1) = x(n) + (\delta i_{L1}(n) + \delta i_{L2}(n)) \tag{21}$$

Now that the controller was defined, the controller gains can be computed; it is important to guarantee the stability in terms of the Lyapunov stability theorem [24] (Section 7.4).

Using Equations (18), (20) and (21) the new extended state-space model can be formulated as:

$$\begin{bmatrix} x(n+1) \\ \delta i_{L1}(n+1) \\ \delta i_{L2}(n+1) \\ \delta v_{C1}(n+1) \\ \delta v_{C2}(n+1) \end{bmatrix} = \underbrace{(A - BK)}_{=:\widetilde{A}} \begin{bmatrix} x(n) \\ \delta i_{L1}(n) \\ \delta i_{L2}(n) \\ \delta v_{C1}(n) \\ \delta v_{C2}(n) \end{bmatrix} \tag{22}$$

where $K = [k_1\ k_2\ k_3\ k_4\ k_5]$ are the controller gains. If the system is characterized with the matrix $\tilde{A}_j$. As recalled in [24] (Th. 7.4.4, pp. 263–264), then it is asymptotically stable if a symmetric matrix $P > 0$ exists, in a way that

$$Q := \widetilde{A}^T P \widetilde{A} - P < 0 \tag{23}$$

The simultaneous computation of P and the controller gains can be obtained by iterative algorithms (see [25]), which is a straightforward matter for solvers such as Yalmip.

6. Fuel Cell Mathematical Model

The realization of the fuel cell model is based on the Nernst reversible voltage equation and is composed of four voltage stages [26–28], i.e.,

$$V_{fc} = E_{Nernst} - V_{act} - V_{conc} - V_{ohm} \tag{24}$$

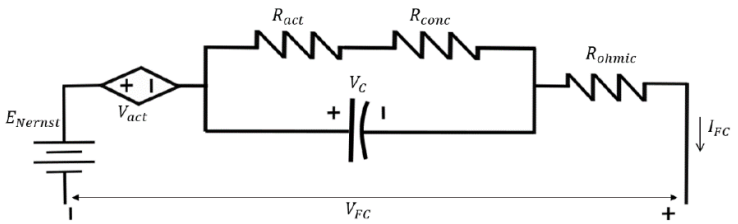

Figure 4. Electrical circuit model of the PEMFC (Proton-Exchange Membrane Fuel Cell).

The Nernst voltage or the reversible voltage corresponds to the potential at the output of the FC without load. In [28] is presented a modified version of the equation of this voltage drop with a term that takes into account the temperature, while P_{O2} and P_{H2} are the partial pressures of oxygen and hydrogen, respectively. The equation from [28] is:

$$E_{Nernst} = 1.229 - 0.85\times10^{-3}\left(T - 298.15\right) + 4.31\times10^{-5}T\left[\ln\left(P_{H2}\right) + \frac{1}{2}\ln\left(P_{O2}\right)\right] \tag{25}$$

where T is the temperature.

Activation voltage losses have a greater impact when low currents circulate through the cell [29].

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where T is the temperature.

Activation voltage losses have a greater impact when low currents circulate through the cell [29]. The Tafel equation is employed to describe the connection between current density and activation losses. This equation is valid if $i > i_o$.

$$V_{act} = -[\xi_1 + \xi_2 T + \xi_3 T \ln C_{O2} + \xi_4 T \ln(I_{FC})] \quad (26)$$

where V_{act} represents the activation loss, T is the temperature of the fuel cell, I_{FC} is the fuel cell current, and the ξ's represent the parametric coefficients for each cell model, the oxygen concentration C_{O2} can be calculated as:

$$C_{O2} = \left(\frac{P_{O2}}{5.08 \times 10^6 e^{\frac{-498}{T}}}\right) \quad (27)$$

Concentration or diffusion losses occur when there is a change in the concentration of reactants, on the contrary of the activation losses, this has a greater impact at very high current, according to the following equation

$$V_{conc} = -B \ln\left(1 - \frac{J}{J_{\max}}\right) \quad (28)$$

where V_{conc} represents the concentration loss, B is a parametric coefficient which depends on each cell, J is the current density of the fuel cell, and $J_{\max}$ is the maximum current density of the fuel cell.

The ohmic losses occur because of electrode resistance, current collectors, and polymeric membrane. They are proportional to the current that circulates in the fuel cell.

$$V_{ohm} = I_{FC}(R_M + R_C) \quad (29)$$

where V_{ohm} represents the ohmic losses, I_{FC} is the fuel cell current, R_C is the resistance of the transfer of protons through the membrane with a value of 300 μΩ and R_M is the resistance of the membrane calculated by:

$$R_M = \left(\frac{\rho_M l}{A}\right) \quad (30)$$

The polarization curve of the fuel cell is shown in Figure 5. This type of graphic indicates the different voltages in the fuel cell model (see Figure 4) vs. the current density [30]. When the current density at the fuel cell changes, the Nerst voltage stays constant, but the fuel cell voltage V_{FC} decreases as the current density is increasing. The different voltage drops—activation, concentration, and ohmic losses are also represented in Figure 5, to have an idea of their behavior. The parameters of the Avista fuel cell stack 500 W are shown in Table 1.

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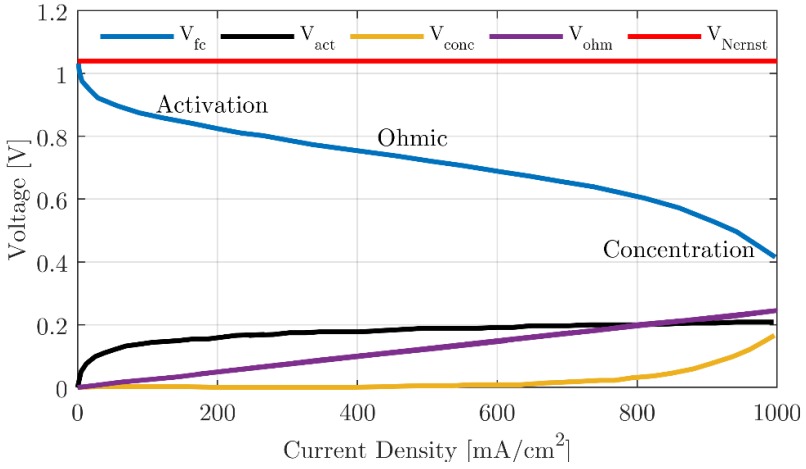

Figure 5. Polarization curve of the PEMFC.

Table 1. Avista 500-W Fuel Cell stack parameters.

Param.	Value	Param.	Value
N	32	ξ_1	−0.948
T	333 K	ξ_2	$0.00286 + 0.0002\ln A + (4.3 \times 10^{-5})\ln C_{H2}$
A	64 cm^2	ξ_3	7.6×10^{-5}
L	178 μm	ξ_4	-1.93×10^{-4}
P_{H2}	1 atm	Ψ	23
P_{O2}	0.2095 atm	J_{max}	469 mA/cm^2
B	0.016 V	J_n	3 mA/cm^2
R_C	0.0003 Ω	I_{max}	30 A

7. Experimental Results

In this section, we show the experimental results of the proposed controller using the hardware-in-the-loop FC implementation. In Figure 6, we show a picture of the experimental prototype and the DSP that implements the proposed discrete time input current controller. The full set of parameters of the experimental setup is shown in Table 2.

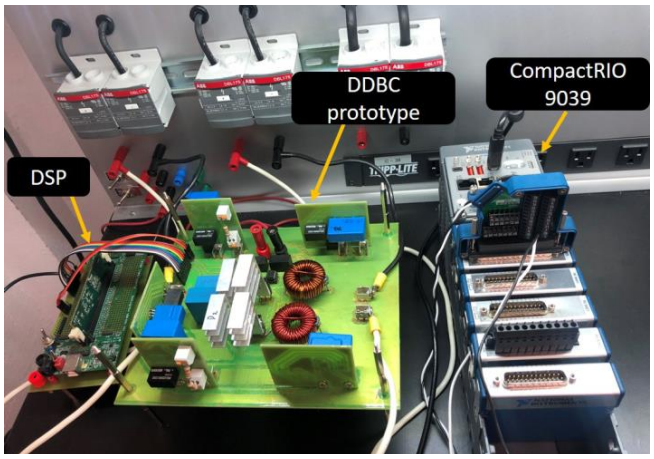

Figure 6. Picture of the implementation of the proposed input current controller.

Table 2. Experimental setup parameters.

Parameter/Component	Value/Information
Maximum power	300 W
Frequency	50 kHz
Input voltage range	20 V–40 V
Output voltage range	80 V–150 V
Converter nominal gain	4
Constant k	0.6
MOSFET S_1 and S_2	IRFP4127 (200V, 75 A)
Diode	LXA20T600 (600 V, 20 A)
Film capacitor C_1	8 μF, 300 V, ESR = 4 mΩ
Film capacitor C_2	4.7 μF, 300 V, ESR = 4 mΩ
Inductor L_1	430 μH, 7 A, ESR = 64 mΩ
Inductor L_2	240 μH, 10 A, ESR = 27 mΩ
Controller gains k_1, k_2, k_3, k_4, k_5	0:0005; 0:0008; 0:0008; 0:0001; 0:0001

We first proceed to validate the hardware-in-the-loop implementation of the FC described in the previous section. In Figure 7, we show the dynamic response of the implemented FC with respect to continuous load variations. Several experimental measurements were performed to validate the corresponding values of the characteristic curve of the FC. These measurements are illustrated in Figure 8. Moreover, experimental measurements of some of the points A, B, and C in Figure 8 are shown in Figures 9–11, respectively.

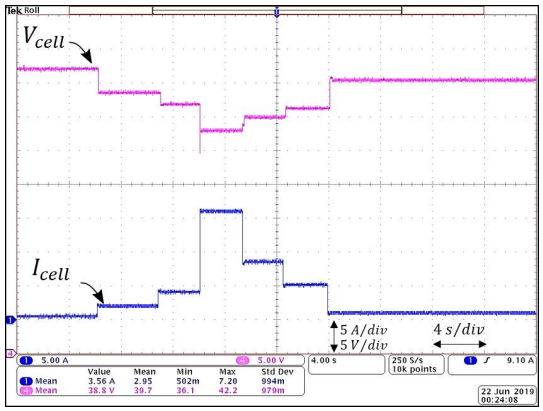

Figure 7. Dynamic response of the Fuel cell (FC) with respect to load variations.

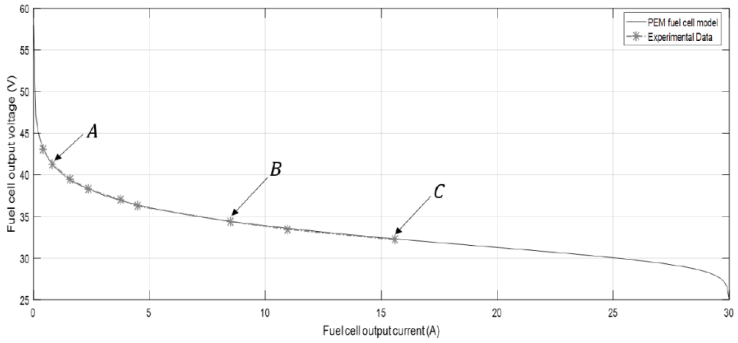

Figure 8. Comparison between experimental and ideal current/voltage values of the implemented FC.

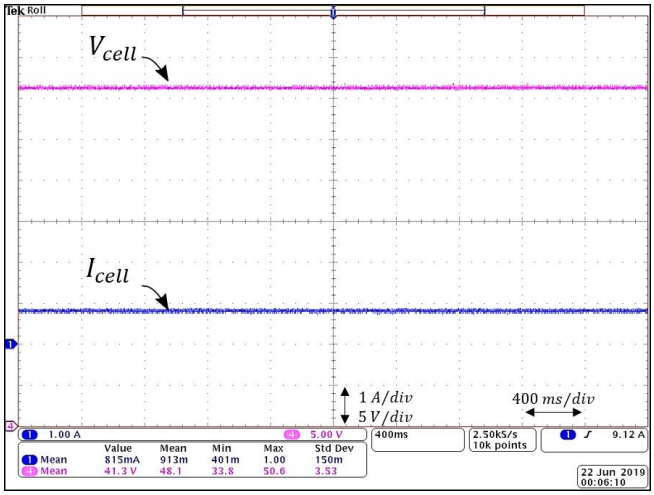

Figure 9. V_{cell} and I_{cell} waveforms corresponding to the A point operating point in Figure 8.

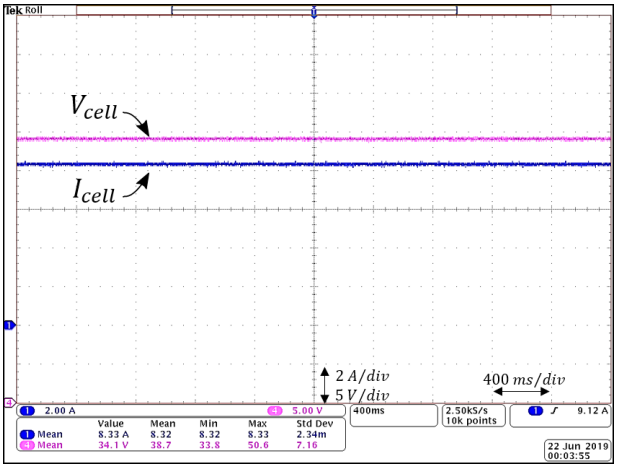

Figure 10. V_{cell} and I_{cell} waveforms corresponding to the B point operating point in Figure 8.

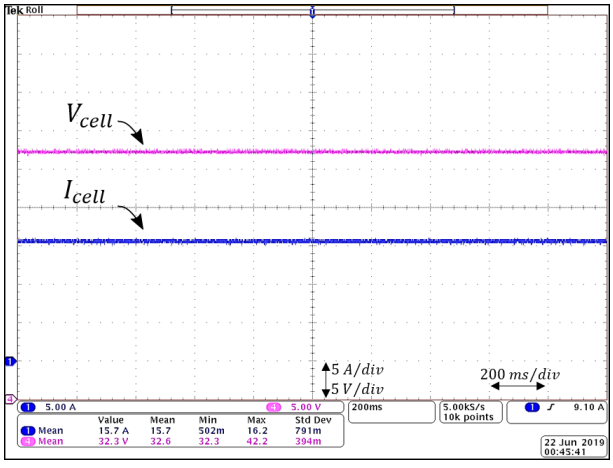

Figure 11. V_{cell} and I_{cell} waveforms corresponding to the C point operating point in Figure 8.

Moreover, additional measurements of the fuel cell are illustrated in Figure 8, where each point (A, B, C, D) corresponds to an operational point of the fuel cell. Points A, B, and C in Figure 8 are shown in Figures 9–11, respectively, which demonstrate that the fuel cell implementation used in this paper corresponds to a real fuel cell.

Experimental results of the proposed current-controller with simultaneous cancellation of input current and output voltage ripples are shown in Figure 12 for an input current set-point of I_{in} = 8 A. As can be seen, the current from both inductors and the input current of the converter (output current of the fuel cell) is shown, the input current (I_{in}) is almost pure DC component; this is the result of the design of the converter and the control loop, which ensures that the duty cycles preserves the relation "k". A comparison between Figure 3, where equal inductors are considered, and Figure 12, where the proposed design and control scheme is employed, the improvement in the input current ripple is clear.

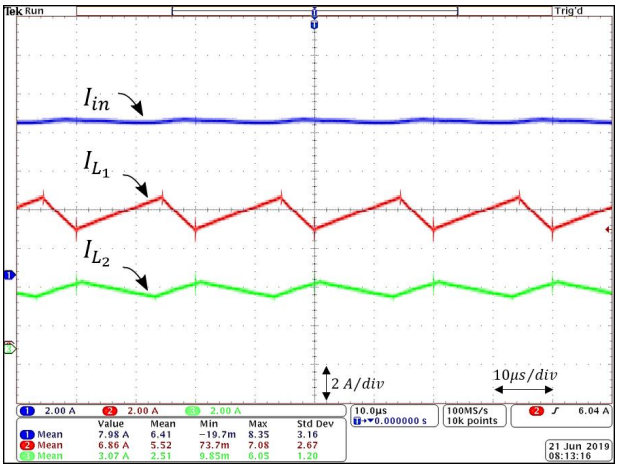

Figure 12. Graphic of currents through inductors and the input under the proposed input current control and ripple cancellation with I_{in} = 8 A as set-point.

Figure 13 shows the output voltage of the converter, the output of each capacitor is shown since capacitors of the prototype have the relation "k" between them, similar to the input current ripple the output voltage (V_{out}) is a pure DC component.

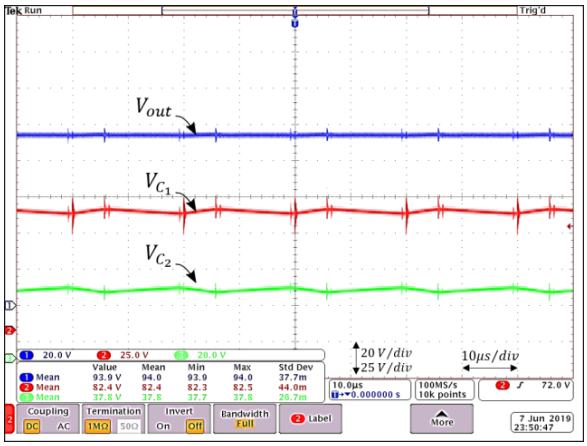

Figure 13. Graphic of voltages across capacitors and the output under the proposed input current control and ripple cancellation with I_{in} = 8A as set-point.

The control over disturbances is demonstrated in Figures 14 and 15; in Figure 14, a step-down voltage of 30% was made; as can be seen, the control ensures that the minimum current ripple is achieved. In Figure 15, a load variation is considered; even when a load variation is present, the current ripple remains at its minimum.

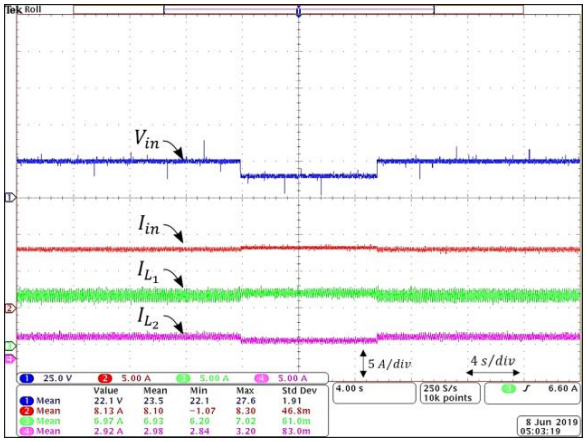

Figure 14. Dynamic compensation of the input current under variations in the input voltage.

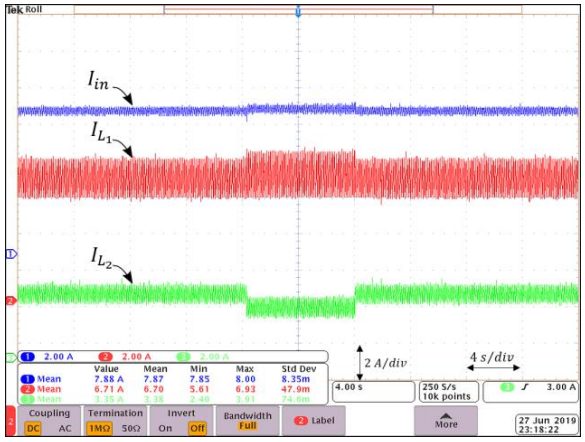

Figure 15. Dynamic compensation of the input current under load variations.

8. Conclusions

This paper presented the implementation of a fuel cell generation system. The base of the designed system is a dc-dc double dual boost converter. The implementation includes the design and experimental validation of the converter, along with the design and validation of a closed-loop digital controller. The designed controller, in coordination with a particular selection of inductors and capacitors, minimizes the switching ripple on the topology, both switching ripples, the input current ripple and the output voltage ripple.

The work includes a complex hardware-in-the-loop experiment, with a fuel cell emulator. The emulator utilizes a controlled power source driven with a CompactRio data acquisition system. The computer program ensures the emulator behaves like a fuel cell. The mathematical model was programmed in LabView. The output of the fuel cell emulator is connected to the double dual boost converter; this particular topology of converter provides a larger voltage gain compared to the traditional boost converter and a smaller input current ripple.

The double dual boost converter was designed with a particular hardware design and operated with a particular PWM; a digital controller was developed for this application and implemented on a Texas Instruments TMS320F28335 digital signal processor.

The full experiment was developed in order to demonstrate that the double dual boost converter under the particular hardware design and the developed digital controller is able to interact with a fuel cell and provides good performance when operated in a fuel cell-based energy generation system.

The developed digital controller considers the relation among duty rations, contributing to the switching ripple minimization in both the input current and output voltage, the control must be

The developed digital controller considers the relation among duty rations, contributing to the switching ripple minimization in both the input current and output voltage, the control must be coordinated with the selection of passive components (inductors and capacitors). This technique encompasses both a design procedure and a PWM strategy for which the designer can freely select the gain at which the input current ripple is canceled. We presented the procedure to achieve this ripple cancellation and showed that an unconstrained selection of the operating region of the converter could be achieved. This technique encompasses both a design procedure and a novel control constraint using the PWM strategy. The control loop was designed considering a small-signal discrete model, and PI converters were tuned according to a Lyapunov stabilization condition that ensures the robustness of the system against disturbances.

The proposed scheme was tested using a fuel cell emulator using Labview in a hardware-in-the-loop fashion. Experimental results from this emulation are presented to corroborate that the behavior is close enough to a real fuel cell. It is demonstrated how the control loop ensures that the ripple mitigation technique is achieved even when the system is subjected to disturbances.

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Chapter 5

Minimum Current-Ripple Point Tracking for Renewable Energy Applications

Summary of the chapter

This chapter presents an article in which a novel output voltage control of a high-gain interleaved DC-DC converter that is able to track a minimum input-current ripple. The controller encompasses three stages: a current stabilization loop, an output-voltage controller and a minimum ripple point tracking control law. The latter is a novel stage that enables a full operating region for which the input-current ripple is minimized. The proposed scheme was validated by implementing experiments in closed-loop operation. In this way, the DDBC is able to both mitigate the harmonic distortion on the current extracted from the PEMFC, which is beneficial to improve the efficiency and life-time of the cell; and on the output-voltage delivered to an output DC bus.

Minimum Current-Ripple Point Tracking for Renewable Energy Applications

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***Abstract*—This paper presents a novel output voltage control of a high-gain interleaved DC-DC converter that is able to track a minimum input-current ripple. The controller encompasses three stages: a current stabilization loop, an output-voltage controller and a minimum ripple point tracking control law. The latter is a novel stage that enables a full operating region for which the input-current ripple is minimized. The proposed scheme was validated by implementing experiments in closed-loop operation. In this way, the DDBC is able to both mitigate the harmonic distortion on the current extracted from the PEMFC, which is beneficial to improve the efficiency and life-time of the cell; and on the output-voltage delivered to an output DC bus.**

***Index Terms*—Interleaved DC-DC converters, renewable energy, current ripple, control, modeling.**

I. Introduction

Renewable energy sources that deliver a low output voltage, according to the requirements of the grid, such as batteries, fuel cells, solar panels, etc., require a DC-DC converter with high input-to-output voltage gain [1], [2].

Also another desirable feature in this DC-DC converters is the high efficiency by avoiding working with extreme duty cycles. Many DC-DC converters have been proposed to step-up voltages. For example, quadratic boost converters (see e.g. [3], [4]); other high-gain topologies based on multilevel stages have been also proposed, see e.g. [5], [6]; high-gain inductor-based topologies, such as switched inductors [7], [8] and coupled inductors [9], [10] are also used.

After weighting the advantages and disadvantages of the above topologies, they all can be considered suitable for renewable energy applications, due to their high-voltage gain. However, input-current ripple is an inherent converter's characteristic [11], which is an issue in such renewable energy applications because this ripple affects them directly in their efficiency and lifetime,(cf. [12]).

This issue has motivated ripple-cancellation contributions based on coupled-inductors (see e.g. [13]) including interleaved topologies (see e.g. [14]). Furthermore, the control design is a relevant issue in DC-DC converters, because the converter has to deal with the input-voltage and load variations that are present in any realistic scenario (see e.g. [15]–[19]). Besides the fact that high-gain and ripple mitigation are topics that may seem apart from each other, some papers studied them on the whole [20]. As can be seen, interleaved converters are a solution for such high-gain and ripple (see e.g. [20]). An ordinary restriction in interleaved converters is their fixed operating point at which the ripple is mitigated. A result of this, is that the duty cycle and gain of the converter is restricted, therefore the current ripple cancellation is poor operating in a different point than the design one.

For instance, a linear controller with a constraint point of operation is proposed in [15]; equal duty cycles is a constraint in [16], in which a linear controller is implemented for a double-dual boost; similarly, with equal inductors a perfect cancellation with a linear controller at a restricted point of operation is presented in [17]; a closed loop controller is implemented in [18], with the same characteristic of equal duty cycles; and [19] presents a linear control for which duty cycles are required to keep a proportional value.

From the literature review, it is clear that high-voltage gain converters, input-current mitigation and their control are relevant issues for which there is still room for improvement.

For this reason, this paper show that it is feasible to achieve a single implementation of a closed-loop high gain interleaved DC-DC converter, overcoming disadvantages of some high-gain topologies, and featuring input-current ripple mitigation at any desirable operating region.

An active way of minimizing the input current achieved by a control law, considering a proper sizing of the inductors. In contrast with previous approaches (e.g. [15]–[19]), the proposed controller is nonlinear; consequently its performance is guaranteed over a full operation range.

In particular, a new closed-loop strategy that is able to simultaneously regulate the output-voltage, and mitigate the input-current ripple is proposed. In order to do so, a concept of *minimum ripple point tracking (MRPT)* for interleaved converters is used. This concept, is presented first in [21], where a three stages controller is presented, an a linear controller is implemented.

In sharp contrast with such contributions, a control scheme

that mitigates harmonic distortion by steering duty cycles to a particular steady-state value is proposed, using a state space nonlinear structure as a modeling specification, that involves the minimum possible current-ripple with respect to any operating point of a voltage-regulated converter. Control scheme and theory demonstrations are validated via experimental results.

II. Interleaved Multilevel Boost Converter

This paper uses an interleaved multilevel boost converter based on the topology proposed in [22] shown in Fig. 1a) and a multilevel version of the converter proposed in [23], which is shown in Fig. 1b). These are topologies based in step-up converters in combination with a capacitor-diode arrangement which function as a multiplier.The main advantages of these arrangement is the capacity to obtain high output voltages with small components, hence with a small size. By interleaving the configurations the topology in Fig. 2 is obtained. To model these topologies there are several changes that need to be considered, one associated to the increased number of stages that imply also and increased number of equations; and a second issue related to switched-capacitor dynamics, which cannot be modeled right away by *averaging* (cf. [24]).

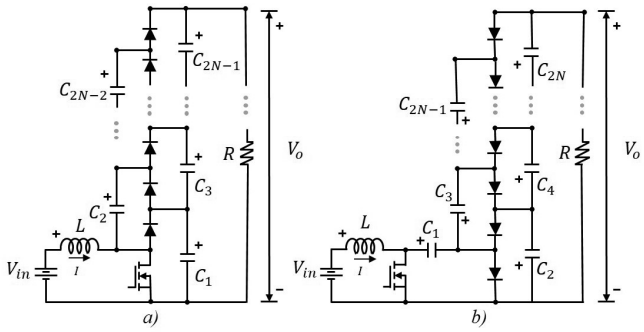

Fig. 1. a) Multilevel Boost Converter b) Three-switch Multilevel Boost Converter

The modelling of a switched-capacitor based for control purposes involve several challenges, one associated to the increased number of stages that impply also and increased number of equations; and a second issue related to switched-capacitor dynamic, which cannot be modelled right away by averaging. Considering that, a large-signal modeling scheme, that will be eventually validated in closed loop operation, is proposed. For instance, an average-loss approach to model the converter in Fig.1 a) can be used as in [19], where equivalent *switch resistances* denoted by R_{eq_i} are used.

In [19], N refers to the number of levels of each converter, and R_{eq_i} is used to express the average losses due to the energy transfer between capacitors (see [25]). Due to the resultant complex expression for the model, a reduced-order model is proposed. In this model it is assume that every capacitor has the same value C, i.e. $C_i := C$, $i = 1, 2, ...$; and that the average voltage across capacitors is always the same, thanks to

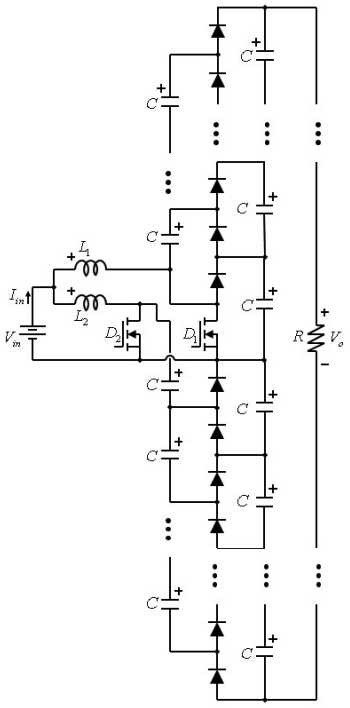

Fig. 2. Interleaved Converter

the inherent voltage balancing of the converter this is perfectly justified (see [26]). Hence, a reduced-order model is obtained by considering

$$V_o = \sum_{k-1}^{N} V_{C(2k-1)} \; ; \;\; V_1 \simeq V_2 \simeq \cdots \simeq V_{C_{2N-1}} \; . \qquad (1)$$

As a result, the derivative of the voltage across the capacitors that serve as energy transfer elements, which is a common assumption when the switching frequency is sufficiently high. Then by adding up the equations of the output capacitors, the model can be reduced to

$$\begin{aligned} L\frac{d}{dt}i &= V_{in} - (1-D)V_{C_1} \; , \\ \sum_{k=1}^{N} C\frac{d}{dt}V_{C_{(2k-1)}} &= (1-D)i - \frac{1}{R}\sum_{k=1}^{N} V_{C_{(2k-1)}} \; . \end{aligned} \qquad (2)$$

By considering (1), equations (2) can be expressed as

$$\begin{aligned} L\frac{d}{dt}i &= V_{in} - \frac{(1-D)}{N}V_o \; , \\ NC\frac{d}{dt}V_o &= (1-D)i - N\frac{V_o}{R} \; . \end{aligned} \qquad (3)$$

In (3) the model proposed is similar to the boost converter steady state equations, i.e. such classic model corresponds to the special elementary case $N = 1$. Under the same considerations, a similar reduced order model for the converter of Fig. 1b) is obtained. It can be easily verified that both models have identical structure. Consequently for ease of

exposition, an index term $j = 1, 2$ to emphasize the duality of the models is used. Hence obtaining

$$\begin{aligned} L_j \frac{d}{dt} i_j &= V_{in} - \left(\frac{1 - D_j}{N_j}\right) V_j \ , \\ N_j C \frac{d}{dt} V_j &= (1 - D_j) i_j - N_j \left(\frac{V_o}{R}\right) \ ; \end{aligned} \tag{4}$$

with $j = 1, 2$. Moreover, the *total input-current* as the sum of the input-current through both converters and an analogous definition for the case of the output voltage is defined, i.e. $I_{in} := i_1 + i_2$ and $V_o := V_1 + V_2$ respectively.

Then the gain of the converter is given by

$$G := \frac{N_1}{1 - D_1} + \frac{N_2}{1 - D_2} \ . \tag{5}$$

A. Sizing of the inductors

The principal reason to consider interleaved converters is their possibility to mitigate the input current ripple. In this paper this task is achieved by a proper sizing of the inductors, and it is show how this selection method is applicable to any operating point. Consider an interleaved converter as in Fig. 2, their triggering signals are 180º phase from each other. In this way, the total input current is the sum of both converters, in this way the ripple can be expressed as $\Delta I_{in} = \Delta i_1 - \Delta i_2$, i.e.

$$\Delta I_{in} = \frac{V_{in} D_1}{f_s L_1} - \frac{V_{in} D_2}{f_s L_2} \ . \tag{6}$$

In order to achieve perfect ripple cancellation, i.e. $\Delta I_{in} = 0$, from (6), it is concluded that

$$L_2 = L_1 \left(\frac{D_2}{D_1}\right) \ . \tag{7}$$

In this paper, this current ripple cancellation approach to the design of converters is the pivotal figure of the proposed *minimum ripple point tracking (MRPT)* control technique. In the following section the details of the closed-loop analysis are introduced. Note that (6) is satisfied either by constraining the duty cycles (and consequently the converter's gain), as usually done in interleaved converters, or by selecting any pair of arbitrary duty cycles and computing the corresponding value of L_i, $i = 1, 2$. This yields a design approach that does not restrict the gain of the converter and permits to select freely the operating point at which $\Delta I_{in} = 0$. This idea was presented in an open loop operation before in [27], the main advantage against traditional ripple cancellation techniques is illustrated in Fig. 3, where a freely selected gain that involves $D_2 = 0.713$ as a given specification can be selected. Around a preselected region, the improvement of using different inductors with respect to the percentage of current-ripple that is obtain by the traditional approach is significant.

In this paper, this current ripple cancellation approach to the design of converters is the pivotal figure of the proposed *minimum ripple point tracking (MRPT)* control technique. In the following section the details of the closed-loop analysis are introduced.

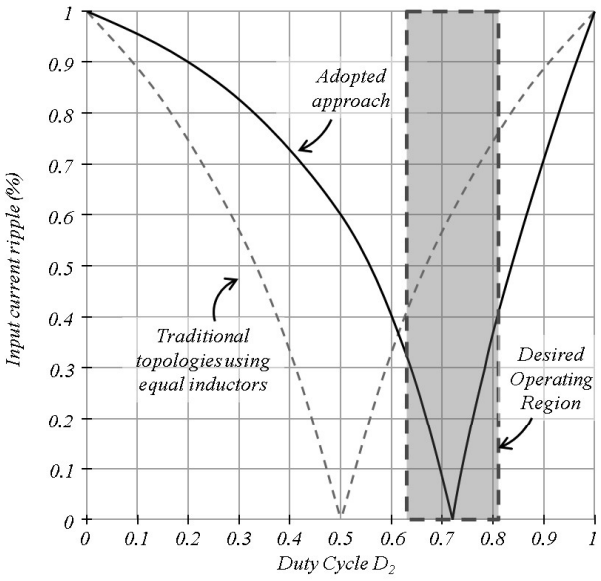

Fig. 3. Ripple level comparison under different design conditions

III. Current and voltage control design

The reduced-order model presented in Section II enables the design of a nonlinear controller. In the following, an *input-output feedback linearization* (cf. [28]) that will be instrumental for the development of our full control scheme is presented. First, by using the following state space nonlinear structure as modeling specification.

$$\begin{aligned} \frac{d}{dt} x &= f(x) + g(x) u \ , \\ y &= h(x) \ . \end{aligned} \tag{8}$$

Note that the derivative of y in (8) can be computed as

$$\frac{d}{dt} y = \underbrace{\frac{\partial h(x)}{\partial x} f(x)}_{L_f h(x)} + \underbrace{\frac{\partial h(x)}{\partial x} g(x)}_{L_g h(x)} u \ . \tag{9}$$

where $L_f h$ and $L_g h$ denote the *Lie derivative* of h along f and g respectively (see [28]). Note that if $L_g h(x) = 0$, the resulting description of the output y does not depend on input u. Consequently, in order to obtain an input-output description the process must be repeated until the input appears in the equation, e.g. by computing a second derivative of y as

$$\frac{d^2}{dt^2} y = \frac{\partial L_f h}{\partial x} \left[f(x) + g(x) u \right] = L_f^2 h(x) + L_g L_f h(x) u \ . \tag{10}$$

A generalized form of equation (10) is given by

$$\frac{d^\rho}{dt^\rho} y = L_f^\rho h(x) + L_g L_f^{\rho - 1} h(x) u \tag{11}$$

where ρ is called *relative degree* and $L_g L_f^{\rho - 1} h(x) \neq 0$. From equation (11) it is easy to verify that selecting the input

$$u := \frac{v - L_f^\rho h(x)}{L_g L_f^{\rho - 1} h(x)} \ , \tag{12}$$

then the following linear input-output expression is obtained

$$\frac{d^\rho}{dt^\rho} y = v \ , \tag{13}$$

where v can be selected as a new input that is defined e.g. by a linear controller. In order to apply this theory to the interleaved topology under study, (4) is expressed as in (8), with $u_j := D_j$, $x_j := \begin{bmatrix} i_j & V_j \end{bmatrix}^\top$, $j = 1, 2$, and

$$f_j(x_j) := \begin{bmatrix} \dfrac{V_{in}}{L_j} - \dfrac{V_j}{N_j L_j} \\ \dfrac{i_j}{N_j C} - \dfrac{V_o}{RC} \end{bmatrix} \ ; \ g_j(x_j) = \begin{bmatrix} \dfrac{V_j}{N_j L_j} \\ -\dfrac{i_j}{N_j C} \end{bmatrix} \ . \tag{14}$$

A. Current Control

Although, for practical purposes, the variable to remain constant under disturbances is the output voltage of the converter, it is well-known that boost converters have *non-minimum phase characteristics* with respect to such variable, i.e. the output voltage cannot be directly controlled (see [24], [29] for further details). Alternatively, the input-current is stabilize to ensure stability. For this reason the selected output of each converter is selected as $y_j := h_j(x_j) = i_j$, with $j = 1, 2$. Then, using (12) and (14), the duty cycle of each converter can be defined as

$$D_j := \frac{N_j}{V_j} \left(u_j L_j - V_{in} + \frac{V_j}{N_j} \right) \ ; \tag{15}$$

with $0 \leq D_j \leq 1$ and $j = 1, 2$. Consequently, the equations that describe the input-current through each converter can be expressed as

$$\frac{d}{dt} i_j = u_j \ ; \quad j = 1, 2 \ . \tag{16}$$

The new inputs u_j, $j = 1, 2$, can be generated by *feedback PI controllers* defined by

$$\begin{aligned} \frac{d}{dt} \overline{x}_j &= i_j - i_{ref_j} \ , \\ u_j &= -k_{1_j} i_j - k_{2_j} \overline{x}_j \ . \end{aligned} \tag{17}$$

where $\overline{x}_j$ denotes the state variable of the integrator of each controller; k_{1_j}, k_{2_j} are the controller gains; i_{ref_j} is the input-current reference for each converter; and $j = 1, 2$.

Note that the value of the gains k_{1_j}, k_{2_j}, $j = 1, 2$, can be computed in a standard way for linear systems, for example since (16)-(17) can be expressed as

$$\frac{d}{dt} \begin{bmatrix} i_j \\ \overline{x}_j \end{bmatrix} = \underbrace{\begin{bmatrix} -k_{1_j} & -k_{2_j} \\ 1 & 0 \end{bmatrix}}_{A_j} \begin{bmatrix} i_j \\ \overline{x}_j \end{bmatrix} - \begin{bmatrix} 0 \\ 1 \end{bmatrix} i_{ref_j} \ ; \ j = 1, 2 \ ; \tag{18}$$

it is enough to select k_{1_j}, k_{2_j} in such a way that the matrices A_j, $j = 1, 2$, have stable eigenvalues (see [24], [29]). In order to add further performance specifications such as the time response of the converters, the *time constants* τ_j, $j = 1, 2$ are considered, and the eigenvalues of A_j as $\sigma_j := 1/\tau_j$, $j = 1, 2$ are defined.

As discussed in Sec. II-A, it is possible to choose different inductances for our implementation, which implies that the converters that are being interleaved have in general different natural time-constants. Consequently, the time-constant of the controllers can be selected taking into account this characteristic in the following way. If it is assume that both switches in Fig. 2 remain closed, which corresponds to the fastest possible way to achieve any given input-current value as reference, the corresponding time-constants can be obtained from the following implication.

$$L_j \frac{\Delta i_j}{\Delta t_j} = V_{in} \implies \Delta t_j = \frac{L_j}{V_{in}} \Delta i_j \tag{19}$$

where Δi_i represents the change in the charging current with respect to the difference of time Δt_j; and $j = 1, 2$. According to (19) the controllers time-constant, represented by τ_j, $j = 1, 2$, must satisfy $5\tau_j \geq \Delta t_j$. Given this relation, the *pole-placement* technique can be applied to compute the feedback gains k_{1_j}, k_{2_j}, $j = 1, 2$ for the current loops.

B. Output Voltage Control

Once the input-current of the converters is on a stable condition, the output voltage can be regulated (see [24], [29]). From this viewpoint, it is desirable to define a further control action by regulating the value of each current-source to achieve a desired output voltage value. In order to do so, the current control loop is extended by implementing the following controllers

$$\begin{aligned} i_{ref_j} &= -g_{1_j} V_j - g_{2_j} z_j \ , \\ \frac{d}{dt} z_j &= V_o - V_{ref} \ . \end{aligned} \tag{20}$$

where g_{1_j}, g_{2_j} are the output-voltage control gains; z_j is the state variable of each of the integrators; V_{ref} is the desired reference for the output voltage; and $j = 1, 2$. These feedback gains are set in an analogous way as in the case of the current-control loops.

IV. Minimum Ripple Point Tracking

Based on the theory discussed in Sec. II-A, an implementation that adds additional constraints to the controllers is proposed, to achieve input-current stabilization and output voltage control, featuring the least possible percentage of current-ripple at any operating point.

First, consider an interleaved converter whose inductances satisfy *by design* the relation given in (7) and whose PWM carriers are in counter-phase. Then, define the following relation

$$k := \frac{L_1}{L_2} = \frac{D_1}{D_2} \ . \tag{21}$$

For the MRPT application it is considered that the relation between inductors size and duty cycles must be equals at all time from equation (21), which establishes the duty cycle relation as

$$D_1 = k D_2 \ . \tag{22}$$

Equation (22) means that the rising slope for both inductors have the same value, and as a consequence for not being complementary, during a period of time, both switches are on

or off, for that reason a small amount of ripple is present in the input current, though it is always less than in the case of complementary duty cycles. In Fig. 4 some curves are shown, that according to the design parameter k, express the minimum ripple point and how the ripple level increases only slightly when moving away from a desired operating region. The MRPT technique follows a specific curve according to the k selected. Using this curve according to a selected minimum ripple point, the design of the converter has a significant advantage over traditional approaches, which is the small amount of ripple on the input current. Furthermore, the main condition (22) can be achieved by a control technique that follows the curve.

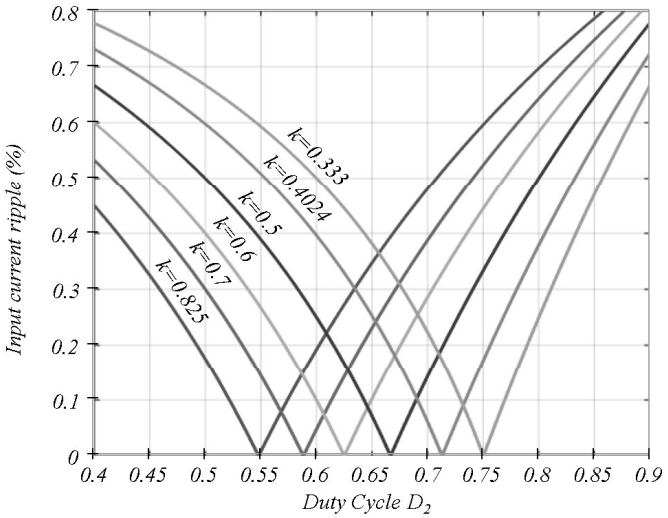

Fig. 4. MRPT curves according to inductors relation

For the MRPT application a nonlinear controller is considered for each multilevel converter and an additional steady-state condition that satisfies (22). In other words, the MRPT technique is accomplished in a steady state, i.e. during the dynamic state, the ripple is not minimized in order to reach the output voltage reference, which makes the converter robust against disturbances, while a minimum ripple point is gradually achieved with time.

Now the improvement obtained with the MRPT technique against a linear control technique is presented, in which complementary duty cycles are considered, this comparison is shown in Fig. 3. Both techniques have equal minimum ripple point. It can be appreciated that when moving from that design point the MRPT technique carries the ripple level to a less percentage in comparison with the linear control.

A. MRPT control loop

When the output voltage has reached the set-point, the MRPT control steers the duty cycles to a point of operation that satisfies the condition (22). This is accomplished by setting the MRPT controller gains slower than the current and output voltage controllers. That is, the controller priority as Current Control $\rightarrow$ Voltage Control $\rightarrow$ MRPT implementation via a suitable selection of controller time-responses.

During this third phase of the controller, the incorporated condition for the current control loop is that duty cycles must satisfy the relation k, expressed in equation (22), which in terms of an integrator can be expressed as follows.

In order to implement the third stage of the controller the following control law is introduced

$$\frac{d}{dt}w = D_1 - kD_2 \tag{23}$$

where w is the variable that implements the *minimum ripple point tracking error*. In order to take advantage on the dynamic of each converter a controller for each one is designed, as a result of this, to get a proper response from the converter the sign of w of the converters are opposite as shown in equation (24), in that way, the fastest converter tends to reach a lower duty cycle value and vice-versa. The current controller with the integrator for the MRPT is expressed in equation (24). Then an additional element to the output-voltage loops in (20) is included as

$$\begin{aligned} i_{ref_1} &= -g_{1_1}V_1 - g_{2_1}z_1 + g_3 w \ , \\ i_{ref_2} &= -g_{1_2}V_2 - g_{2_2}z_2 - g_3 w \ ; \end{aligned} \tag{24}$$

Note that given (24), the current set-point is a function of the output voltage value and the MRPT error. The full schematic of the controller is illustrated in Fig. 5.

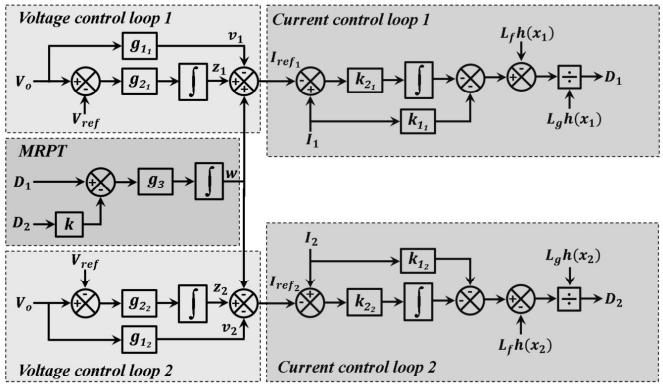

Fig. 5. Control Loop

V. Experimental results

In order to validate the proposed controller an experiment was carried out on a four-level version of the converter, i.e. $N_1 = 2$ and $N_2 = 2$. The experiment was performed using a prototype of the converter, an electronic load and a digital signal processor TI TMS320F28335 for the closed loop implementation. The prototype/controller parameters are summarized in Table I.

The controller was tested under input voltage step variations, and abrupt load changes.

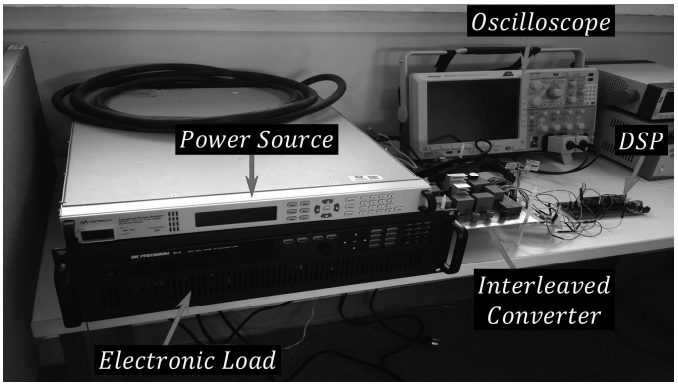

Fig. 6. Interleaved converter prototype

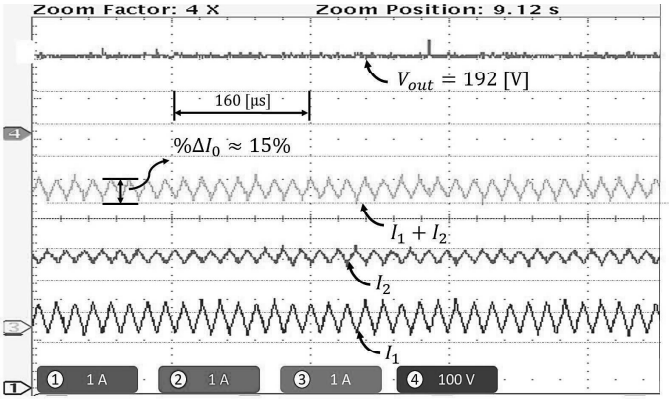

Fig. 7. Closed-loop operation using the traditional approach

TABLE I
DATA OF THE EXPERIMENT

Parameter	*Value*
L_1	*330 µH*
L_2	*820 µH*
C	*10 µF*
Mosfets	*IRFP250*
Diodes	*BYW29E-400*
Resistance	*500 Ω*
N_1, N_2	*2*
F_s	*50 kHz*
V_{in}	*24 V*
V_{out}	*192 V*
k_{1_1}, k_{1_2}	$-5e^3$
k_{2_1}	$-5e^4$
k_{2_2}	$-5e^2$
g_{1_1}	$-\frac{1}{100}$
g_{1_2}	$-\frac{1}{50}$
g_{2_1}	$-\frac{1}{300}$
g_{2_2}	$-\frac{1}{800}$
g_3	$\frac{1}{80}$

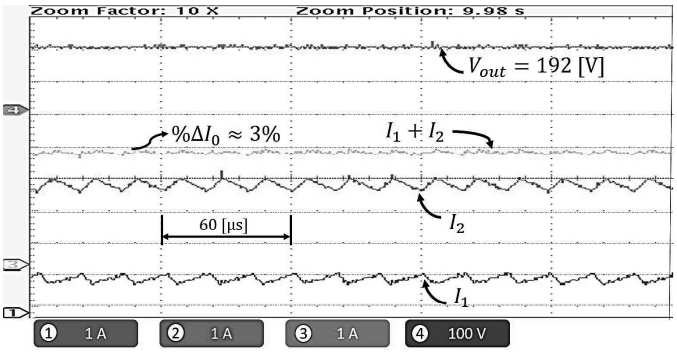

Fig. 8. Topology working with the MRPT controller

A. Steady-state validation

As stated on previous sections, important advantages of this topology include a high gain and ripple cancellation; consequently, experimental validation of both features are presented. Moreover, the principal benefit of the proposed controller, is its flexibility over the operational point while searching a minimum ripple condition. In order to provide a fair comparison, a controller featuring the traditional approach is implemented, using the same converter as in [19]. In this way, it is corroborate that the proposed MRPT control strategy produces minimized values. Considering this, the topology is operated far away (i.e. $V_{set-point} = 192$) from the design point ($V_{design} = 230V$). The results using a traditional control technique with a traditional approach (with constrained duty cycles) is shown in Fig. 7. As expected, the total input current (green line) has an excessive ripple level, nearby to a 15% of the input current value.

Using the same reference for the output voltage, the new MRPT controller is implemented. Experimental results are shown in Fig. 8. The implementation of the MRPT control accomplished a ripple value nearby to 3% percent.

B. Dynamic (tracking) validation

In Fig. 9, the experimental validation for the MRPT theory is presented in dynamical terms. Due to the big difference between the set-point and the instant voltage value, the controller, having a quick response, carry the duty cycle of the fastest controller to a high value, giving a time to the other converter to reach the set-point. This case, where duty cycles cross their respective values is so particular, however, when turning on the converter it can be appreciated. Fig. 9 has four traces, the blue line corresponds to the current of the upper converter (the one in Fig. 1 a)), which in our prototype is the fastest converter. The red line corresponds to the other converter (the one in Fig. 1 b)) that constitutes the overall interleaved topology. The total input current is marked in green, and the output voltage is presented as a purple line. It is easy to verify that during the dynamic state, the upper converter current takes a higher value than the one in steady state. Note also that the total input-current ripple is dynamically mitigated as t increases, i.e. the converter is tracking the point of minimum ripple, while the output voltage is able to reach the set-point simultaneously. Finally, in steady state the converter remains under a minimum ripple condition.

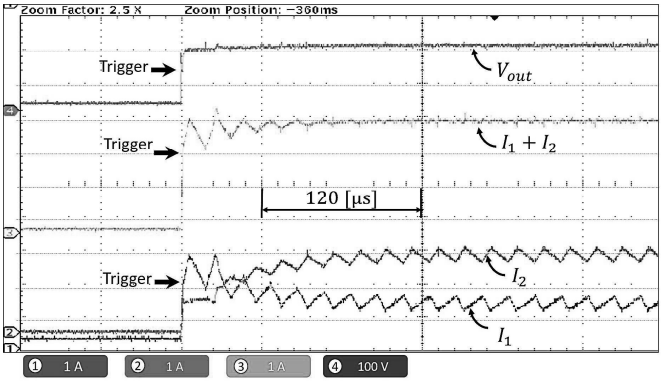

Fig. 9. MRPT experimental validation

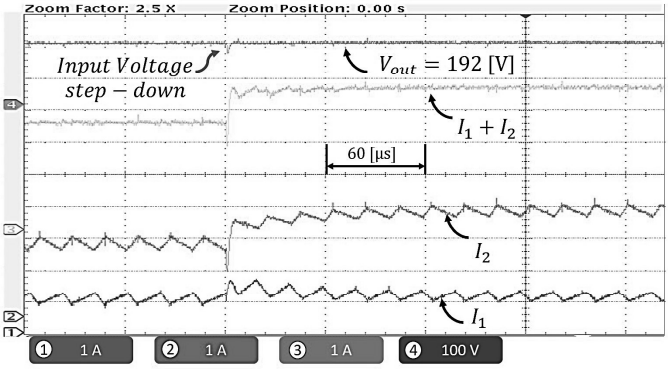

Fig. 11. Controller action under a voltage-step

C. Control validation under disturbances

Since a controller must be capable to provide a quick response under disturbances that may affect the output voltage, e.g. load changes or voltage input changes; these scenarios are also validated. Fig. 10 depicts the controller action when a load change is applied to the converter, in this case, the resistance value is dropped from 1200 Ω to 400 Ω. Note that one converter is always faster than the other in order to achieve the fastest possible response against disturbances.

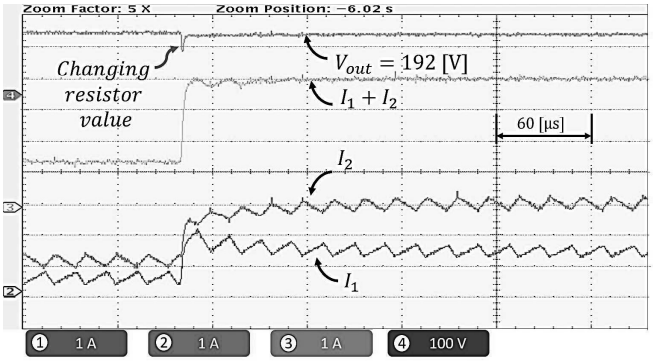

Fig. 10. Controller action under a load change

In Fig. 11 a voltage step down of 20% V_{in} was applied to the converter. A similar compensating behavior, as in the load-change case, is observed on the input currents.

VI. Conclusions

A new control strategy for interleaved converters is introduced, by using a topology with compelling features such as high gain, high efficiency and input current ripple cancellation, which makes it suitable for renewable energy applications. A new approach to current ripple cancellation for which duty cycles are not constrained was adopted. This approach is the pivotal figure of a control technique with an MRPT implementation, which permits a low current ripple level even with a variable operating point. Experimental results proved that the proposed controller allows an output voltage regulation and an input current ripple minimization under disturbances like load changes.

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Chapter 6

Energy Management Strategy for Ultracapacitors in Hybrid Electric Vehicles

Summary of the chapter

This chapter is intended to Electric Vehicles (EV). EV are attracting attention due to their environmentally friendly operation; they market penetration may require the installation of a large number of charging stages, which is expensive and challenging from the logistic point of view. Hybrid electric vehicles HEV, may get charged from different sources which makes a flexible operation, the combination of a fuel cell, a battery, and an ultra-capacitor represents a plausible solution, ultracapacitors provide the power density required for the acceleration, and the fuel cell provides the energy density required to have a good autonomy. This manuscript proposes a fussy-logic-based energy administration strategy for an HEV feed by a set of a fuel cell, a battery, and an ultra-capacitor. The proposed strategy controls the state of charge of the ultra-capacitor, considering their superior energy storage capability. Experimental results demonstrate that the proposed strategy reduces the waste of energy by 14%. This leads to energy savings, the vehicle consumed 218 Wh per km without the proposed strategy against 192 Wh per km without it, for the same example of the driving path; the estimated fuel efficiency increased 96 to 109 miles per gallons.

Energy Management Strategy for Ultracapacitors in Hybrid Electric Vehicles

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***Abstract*—Electric vehicles *EV* are attracting attention due to their environmentally friendly operation; they market penetration may require the installation of a large number of charging stages, which is expensive and challenging from the logistic point of view. Hybrid electric vehicles *HEV*, may get charged from different sources which makes a flexible operation, the combination of a fuel cell, a battery, and an ultra-capacitor represents a plausible solution, ultracapacitors provide the power density required for the acceleration, and the fuel cell provides the energy density required to have a good autonomy. This manuscript proposes a fussy-logic-based energy administration strategy for an HEV feed by a set of a fuel cell, a battery, and an ultra-capacitor. The proposed strategy controls the state of charge of the ultra-capacitor, considering their superior energy storage capability. Experimental results demonstrate that the proposed strategy reduces the waste of energy by 14%. This leads to energy savings, the vehicle consumed 218 Wh per km without the proposed strategy against 192 Wh per km without it, for the same example of the driving path; the estimated fuel efficiency increased 96 to 109 miles per gallons.**

Keywords—Energy administration strategy, hybrid electric vehicle, fussy logic.

I. Introduction

One of the most promising renewable energy sources are Fuel Cells *FCs*, operate with low noise, and their emissions are environmentally friendly they portability and energy density make it a good option for Hybrid Electric Vehicles *HEVs*, among the different types of *FCs*, the ones based on Proton Exchange Membranes *PEM*, utilize an electrolyte membrane made from a solid polymer, their main advantage is their low-temperature operation, PEM-FCs are considered the most suitable for *HEVs* [1]-[3].

Despite the benefits of *PEM-FCs*, it has limitations, such as a slow response to a step demand of power [2]-[5], required for vehicle acceleration; furthermore, they do not support bidirectional power flow, which is a requirement for electric vehicles applications due to the regenerative braking. A feasible solution to the discussed limitation is the combination of the FC with an energy storage device such as capacitors, ultra-capacitors, flywheels, batteries, etc. [6].

Batteries, ultra-capacitors, and other Energy Storage Systems *ESS* can provide a fast response for the vehicle acceleration power demand [6]-[9]. Batteries and ultra-capacitor share some similarities, but batteries have a larger energy density compare to the ultra-capacitors, for the same volume, batteries can provide a larger autonomy, in the other hand, ultra-capacitors have a larger power density, and then can provide faster response, under a step power demand. Ultra-capacitors have a larger useful life compared to batteries, which lose their performance after some thousands of charge-discharge cycles [10], against the one million cycles supported by ultra-capacitors [11].

Several works in state of the art have studied combined systems with fuel cells and batteries, or fuel cells and ultra-capacitors, the main performance indicators studied are fuel economy, performance, optimization during design and control strategy [6-9]. Several configurations of power trains have been also analyzed [12-16]. A system made with a fuel cell combined with a battery or an ultra-capacitor, can provide a high-power density and a high-energy-density, good efficiency and dynamic response, and would be capable of performing the regenerative braking [13]-[20].

The main objectives when hybridizing the power system of an electric vehicle, with fuel cells and an energy storage device is to optimize the volume, weight, cost, acceleration, and autonomy. The energy administration strategy *EAS* is responsible for ensuring their adequate operation [18]-[20], and to coordinate the power system operation with several control loops and the electronic supervisory system [21]-[24].

This paper introduced a new Energy Administration Strategy *EAS* for the power system of an *HEV*; the system is comprised by all three: fuel cell, battery, and ultra-capacitor, the proposed *EAS* is designed for a particular topology in which the ultra-capacitor is directly connected to the direct current *dc* system bus. It aims to control (in an indirect manner) the charge of the ultra-capacitor (by controlling the power flow in the *FC* and the battery) to take advantage of its capability to store energy and to improve the vehicle autonomy. The strategy is based on fuzzy logic. Experimental results demonstrate that the proposed strategy reduces the waste of energy by *14%*. This leads to energy savings, the vehicle consumed *218* Wh per km without the proposed strategy against *192* Wh per km without it, for the same example of the driving path; the estimated fuel efficiency increased *96* to *109* miles per gallons

II. Description of the Systems and Their Requirements

Fig. 1 shows a diagram of the power system under study, the battery and the *FC* have their own dc to dc converter to get connected to the main dc bus, which is usual in this kind of applications [25]-[28], in the other hand, the ultra-capacitor is directly connected to the dc bus, the benefits of this interconnection are: *(i)* Since the ultra-capacitor is connected directly, losses for their charge and discharge are minimal. *(ii)* No capacitor bank is required at the dc bus since the ultra-capacitor can store energy and absorb any variation of the dc bus. *(iii)* The direct interconnection of the ultracapacitor ensures their fast interaction with the motor driver, with no delay related to a dc to dc converter.

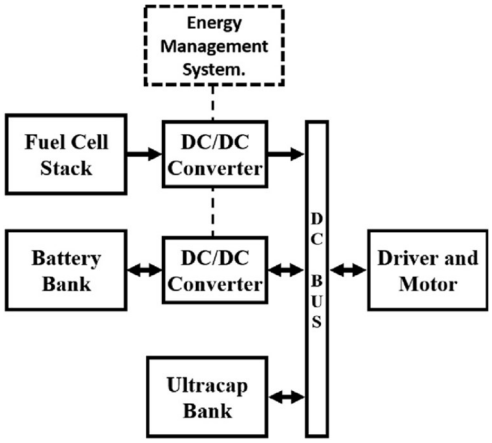

Fig. 1. Hybrid Power system configuration used.

The objective of the *EAS* is controlling the *HEV* energy consumption to have optimal use of the available energy, which is restricted to the hydrogen available quantity, due to the operation of the system with the ultra-capacitor connected to the dc bus, the dc bus voltage requires a range of operation I which the voltage may vary, to take advantage of the charge and discharge of the ultra-capacitor, this variation must be restricted to safe operation for the entire system. The *EAS* would define the long-term utilization of the available energy, including the regenerative braking, and must be able to operate for unpredicted driving paths and conditions. The *EAS* operates by changing some parameters, that are related to the charge and discharge of the battery and ultra-capacitor, and the administration of the energy available from the *FC*, along with the vehicle and driving parameters: the velocity, acceleration, and temperature.

Different *EAS* can be categorized by whether they need future information, which is designated as causal strategies, or non-causal strategies (for those strategies that do not need future information about the power demand). Non-causal strategies may be based on mission profile estimation. Despite the feasibility of non-causal strategies, they are not easy to implement due to their nature and computational cost. The main difficulty is the unpredictable nature of future power demand, a percentage of the demand can be estimated for certain applications, such as delivery vehicles with a well-planned path (including slopes, desired speed, etc.).

Expert-based and heuristic strategies usually have better results under unpredicted or real-time conditions in *EAS*; those kinds of strategies may be implemented with fussy systems based on Boolean-logic. Different objectives can be followed to maximize the performance of the *HEV*, for example: minimizing the hydrogen consumption [4], [6], [7], maximizing batteries lifetime [3], [5], [6], maximizing the use of ultra-capacitors energy [5], [9]. This last goal is of particular interest in this work, since the power system configuration (the ultra-capacitor is connected to the dc bus). The idea of this last strategy is to maintain the ultra-capacitor state of charge at a level in which it can accept or deliver energy.

Therefore, the objective of the proposed *EAS* is taking advantage of the ultra-capacitor capability to store energy and to maintain enough capacity to accept energy during regenerative braking, and enough energy to deliver during vehicle acceleration.

Most battery-powered *EV*, use a depleting-charge strategy, which considers that the final State of Charge *SOC* in the battery is lower than the initial *SOC*. But, for the system shown in Fig. 1, a sustain charge strategy for the ultra-capacitor may be more beneficial, which means the strategy considers ultra-capacitor *SOC* is maintained within a specific range.

III. Proposed Energy Administration Strategy

The proposed *EAS* aims to improve the response of the vehicle under acceleration by maintaining a certain ultra-capacitor *SOC* and by increasing the vehicle autonomy by ensuring the *SOC* level is able to receive energy from the regenerative braking.

The initial step is defining input and output variables for the control system; in this case, the input parameters are the vehicle velocity and the ultra-capacitor *SOC*. Since the ultra-capacitor has no dc to dc converter but a direct connection to the dc bus, their energy must be indirectly controlled by controlling the power interchanged by the fuel cell and the battery. A first Kirchhoff current law expression of the system is (1):

$$i_D(t) = i_{fc}(t) + i_{bat}(t) + i_{uc}(t) \qquad \forall t \qquad (1)$$

Being i_D the current demand, mainly from the motor drive, but includes auxiliary subsystems in the vehicle, i_{fc} is the *FC* current, i_{bat} is battery current, and i_{uc} is the ultra-capacitor current. From (1), the ultra-capacitor current can be expressed as (2):

$$i_{uc}(t) = i_D(t) - \left(i_{fc}(t) + i_{bat}(t)\right) \qquad \forall t \qquad (2)$$

From (2), it can be observed that the current in the ultra-capacitor can be controlled with the current through the battery and the *FC* (the demand cannot be controlled). A scalar factor f_e can be defined to express the percentage of the demand that is cover by the battery and the *FC*.

$$\left(i_{fc} + i_{bat}\right) = f_e \cdot i_D \qquad (3)$$

The rest percentage of the demand, not covered in (3), would be provided by the ultra-capacitor, and then it can be expressed as (4).

$$i_{uc} = (1 - f_e) i_D \qquad (4)$$

The current i_{uc} would depend on f_e and the current demand. If $f_e>1$, i_{uc} becomes negative, and the ultra-capacitor is getting charged, if $f_e<1$, i_{uc} is positive, and the ultra-capacitor is getting discharged. The idea to maintain the ultra-capacitor *SOC* at a defined level to be able to provide or receive energy can be expressed as a balance among the kinetic and electric energy in the vehicle, as is equation (5).

$$E_{uc} + E_{kin} = x \tag{5}$$

Being E_{uc}, the energy stored in the ultra-capacitor, and E_{kin}, the *HEV* kinetic energy, x is a variable defined to balance the equation.

Then we can use input and output variables to implement the *EAS* based on the fuzzy logic theory. That theory was chosen since its heuristic and non-causal nature (ideal for this application).

A. Fuzzy-logic-based system

This section presents the Fuzzy Inference System *FIS*, developed to instrument the proposed *EAS*. Among the different *FIS* available in the literature, such as the Tsukamoto, Mamdani and Sugeno. This work uses the Mamdani *FIS* since its capability to use either numerical data or verbal formulated rules, furthermore, the Mamdani *FIS* has a simple and intuitive implementation and requires a low number of parameters.

A fuzzification process is used to map the input parameters, the vehicle velocity, and the ultra-capacitor *SOC* into fuzzy sets. An inference machine is then used to evaluate the sets with condition-consequence control rules. A fuzzy set is obtained as an output of the evaluation, and it is finally, defuzzied to get a numerical value. The *FIS* output is the scalar factor f_e, used to control the ultra-capacitor *SOC*.

The structure of the *FIS* is composed of a set of rules, a database (containing the Membership Functions *MF*), and a reasoning mechanism (to perform the interpretation of the defined rules) and the given facts to obtain a conclusion or output. The *FIS* rules used were obtained from empirical reasonings about the energy consumption of the system. The postulates are:

(i) If both the velocity and the ultra-capacitor *SOC* are high, f_e must be reduced to reduce the ultra-capacitor *SOC*.

(ii) If both the velocity and the ultra-capacitor *SOC* are low, f_e must be increased to increase the ultra-capacitor *SOC*.

Fig. 2 shows the fuzzy logic process of inference.

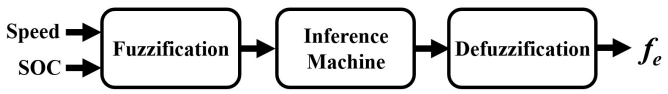

Fig. 2. Process of fuzzy inference.

B. Linguistic input-output variables and numerical ranges

linguistics variables are composed by the variable named x, the set of values $T(x)$, the universe X, the syntactic G which produces $T(x)$ values, and a semantics rule M associated with each linguistic value B where $M(B)$ is a fuzzy set in X.

The used *FIS* contains two input linguistic variables: the *velocity(s)* and the ultra-capacitor *SOC*, a set of linguistic values for those variables can be expressed as (6) and (7), respectively.

$$T(velocity) = \{low, medium, high\}. \quad X_v = [0, 60] \tag{6}$$

$$T(SOC) = \{low, medium, high\}. \quad Y_{SOC} = [0, 100] \tag{7}$$

The output linguistic variable is expressed as equation (8) along with its numerical range.

$$T(scaling\ factor) = \{very\ small, small, medium, very\ big\}. \quad Z_v = [0.5, 1.5] \tag{8}$$

C. Input-output variables Membership Functions MF

The fuzzy sets or *MF* are conventionally provided by mathematical formulas, triangular and trapezoidal; in this case, they are easy to represent and require a low computational effort to get evaluated, and then they are perfect for real-time applications. Each semantic rule defines one *MF* for each linguistic value. In the *velocity* case, the function is expressed as equations (9), (10), and (11).

$$M(Low) = Trapezoidal(x; 0,0,6,27)$$

$$M(Low) = \begin{cases} 0, & x < 0 \\ 1, & 0 \le x \le 6 \\ \frac{27-x}{27-6}, & 6 \le x \le 27 \\ 0, & 27 \le x \end{cases} \tag{9}$$

$$M(Medium) = Trapezoidal(x; 18,27,33,42)$$

$$M(Medium) \begin{cases} 0, & x \le 18 \\ \frac{x-18}{27-18}, & 18 \le x \le 27 \\ 1, & 27 \le x \le 33. \\ \frac{42-x}{42-33}, & 33 \le x \le 42 \\ 0, & 42 \le x \end{cases} \tag{10}$$

$$M(High) = Trapezoidal(x; 33,54,60,60)$$

$$M(High) = \begin{cases} 0, & x \le 33 \\ \frac{x-33}{54-3}, & 33 \le x \le 54 \\ 1, & 54 \le x \le 60 \\ 0, & 60 < x \end{cases} \tag{11}$$

The described *velocity MF* is shown in Fig. 3

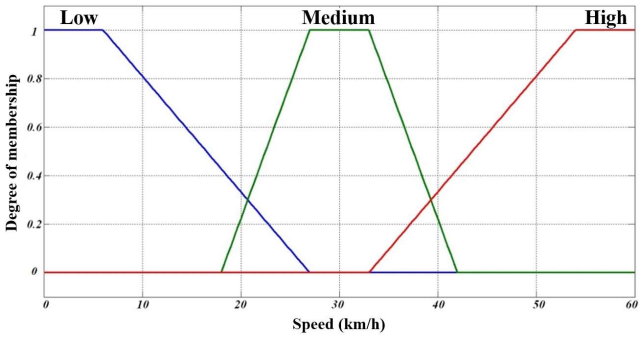

Fig. 3. *Velocity MF* (input variable).

The *MF* of the second input variable, the ultra-capacitor *SOC* was defined as in equations (12), (13) and (14).

$$M(Low) = Trapezoidal(y; 0,0,15,45)$$

$$M(Low) = \begin{cases} 0, & y < 0 \\ 1, & 0 \le y \le 15 \\ \frac{45-y}{45-1}, & 15 \le y \le 45 \\ 0, & 45 \le y \end{cases}. \quad (12)$$

$$M(Medium) = Trapezoidal(y; 25,45,60,85)$$

$$M(Medium) = \begin{cases} 0, & y \le 25 \\ \frac{y-25}{45-25}, & 25 \le y \le 45 \\ 1, & 45 \le y \le 60. \\ \frac{85-y}{85-60}, & 60 \le y \le 85 \\ 0, & 85 \le y \end{cases} \quad (13)$$

$$M(High) = Trapezoidal(y; 55,85,100,100)$$

$$M(High) = \begin{cases} 0, & y \le 55 \\ \frac{y-55}{85-55}, & 55 \le y \le 85 \\ 1, & 85 \le y \le 100 \\ 0, & 100 < y \end{cases}. \quad (14)$$

The described *MF* for the *SOC* is shown in Fig. 4.

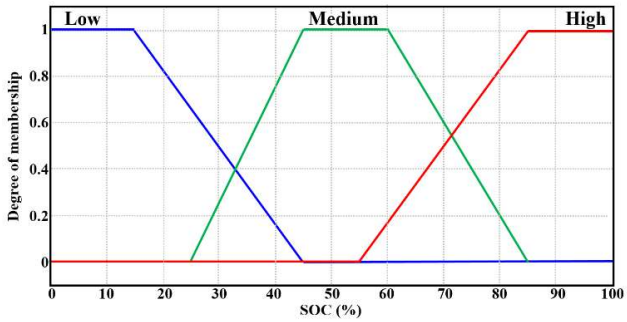

Fig. 4. *SOC MF* (input variable).

Finally, the *MF* assigned to the output linguistic variable "*Scaling factor*" is expressed by equations (15) to (19) and shown in Fig. 5.

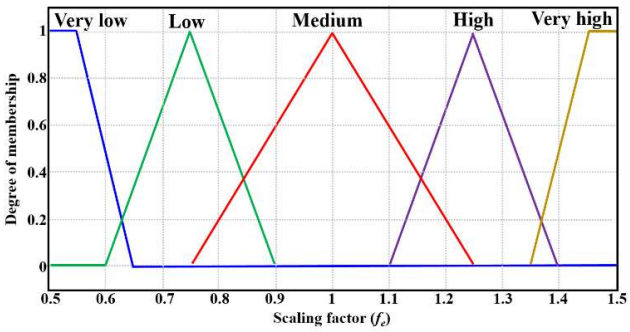

Fig. 5. Membership function of *scaling factor* output variable

$$M(Very\ low) = Trapezoidal(z; 0,0,0.55,0.65)$$

$$M(Very\ low) \begin{cases} 0, & z < 0 \\ 1, & 0 \le z \le 0.55 \\ \frac{0.65-z}{0.65-0.55}, & 0.55 \le z \le 0.65 \\ 0, & 0.65 \le z \end{cases}. \quad (15)$$

$$M(low) = Trapezoidal(z; 0.6,0.75,0.9)$$

$$M(low) = \begin{cases} 0, & z \le 0.6 \\ \frac{z-0.6}{0.75-0.6}, & 0.6 \le z \le 0.75 \\ \frac{0.9-z}{0.9-0.75}, & 0.75 \le z \le 0.9 \\ 0, & 0.9 \le z \end{cases}. \quad (16)$$

$$M(Medium) = Trapezoidal(z; 0.75,1,1.25)$$

$$M(Medium) = \begin{cases} 0, & z \le 0.75 \\ \frac{z-0.75}{1-0.75}, & 0.75 \le z \le 1 \\ \frac{1.25-z}{1.25-1}, & 1 \le z \le 1.25 \\ 0, & 1.25 \le z \end{cases}. \quad (17)$$

$$M(High) = Trapezoidal(z; 1.1,1.25,1.4)$$

$$M(High) = \begin{cases} 0, & z \le 1.1 \\ \frac{z-1.1}{1.25-1.1}, & 1.1 \le z \le 1.25 \\ \frac{1.4-z}{1.4-1.25}, & 1.25 \le z \le 1.4 \\ 0, & 1.4 \le z \end{cases}. \quad (18)$$

$$M(Very\ high) = Trapezoidal(z; 1.35,1.45,1.5,1.5)$$

$$M(Very\ high) = \begin{cases} 0, & z \le 1.35 \\ \frac{z-1.35}{1.45-1.35}, & 1.35 \le z \le 1.45 \\ 1, & 1.45 \le z \le 1.5 \\ 0, & 1.5 < z \end{cases}. \quad (19)$$

D. Fuzzy rules

The *FIS* utilized in this work is based on the enlisted rules, which were selected according to the previously described heuristic of the problem.

If *velocity* is **Low** and *SOC* is **Low**, then f_e is **Very high**

If *velocity* is **Low** and *SOC* is **Medium**, then f_e is **High**

If *velocity* is **Low** and *SOC* is **High**, then f_e is **Medium**

If *velocity* is **Medium** and *SOC* is **Low**, then f_e is **High**

If *velocity* is **Medium** and *SOC* is **Medium**, then f_e is **Medium**

If *velocity* is **Medium** and *SOC* is **High**, then f_e is **Low**

If *velocity* is **High** and *SOC* is **Low**, then f_e is **Medium**

If *velocity* is **High** and *SOC* is **Medium**, then f_e is **Low**

If *velocity* is **High** and *SOC* is **High**, then f_e is **Very low**

Each rule, which has two antecedents, have the form: "if x is A and y is B, then z is C" which can be written as A × B → C.

This can be transformed into a three elements relationship as follows:

$$R_m(A,B,C) = (A \times B) \times C$$

$$R_m(A,B,C) = \int \mu_A(x) \wedge \mu_B(y) \wedge \mu_C(z)/(x,y,z) \ . \quad (20)$$

The resulting set $\boldsymbol{C'}$ can be expressed as:

$$C' = (A' \times B') \circ (A \times B \rightarrow C). \quad (21)$$

The total response is given by:

$$\mu_{C'}(z) =$$

$$\vee_{x,y} [\mu_{A'}(x) \wedge \mu_{B'}(y)] \wedge [\mu_A(x) \wedge \mu_B(y) \wedge \mu_C(z)].$$

$$\vee_{x,y} \{[\mu_{A'}(x) \wedge \mu_{B'}(y) \wedge \mu_A(x) \wedge \mu_B(y)]\} \wedge \mu_C(z).$$

$$\underbrace{\{\vee_x [\mu_{A'}(x) \wedge \mu_A(x)]\}}_{\omega_1} \wedge \underbrace{\{\vee_y [\mu_{B'}(y) \wedge \mu_B(y)]\}}_{\omega_2} \wedge \mu_C(z).$$

$$\mu_{C'}(z) = \underbrace{(\omega_1 \wedge \omega_2)}_{Force} \wedge \mu_C(z). \quad (22)$$

Where $\boldsymbol{\omega_1}$ and $\boldsymbol{\omega_2}$ are the maximum values of the membership functions *MFs* $A \cap A'$ and $B \cap B'$, respectively. $\boldsymbol{\omega_1}$ indicates the compatibility degree among A y A', the same happens for $\boldsymbol{\omega_2}$. Since the antecedent is comprised of the connection "and", $\boldsymbol{\omega_1 \wedge \omega_2}$ is called the fuzzy rule accomplishment degree. The resultant *MF* $\boldsymbol{C'}$ is equal to the *MF* of $\boldsymbol{C}$ cut it by the force $\boldsymbol{\omega = \omega_1 \wedge \omega_2}$.

Since the utilized fussy inference system is made by nine rules, several fuzzy relations must be joined related to them. For instead:

Premise 1 (fact): "x" is A′ and "y" is B′

Premise 2 (rule 1): If "x" is A_1 and "y" is B_1 then "z" is C_1

Premise 3 (rule 2): If xis $A_2$and "y" is B_2 then "z" is C_2

Consequence(conclusion): "z" is C′

To verify this inference procedure, be:

$$R_1 = A_1 \times B_1 \rightarrow C_1$$

$$R_2 = A_2 \times B_2 \rightarrow C_2$$

Being R_1 and R_2 rules *1* and *2*, respectively. The resultant set is expressed as:

$$C' = (A' \times B') \circ (R_1 \cup R_2).$$

$$C' = [(A' \times B') \circ R_1] \cup [(A' \times B') \circ R_2].$$

$$C' = (A' \times B') \circ (R_1 \cup R_2). \quad (23)$$

Where $\boldsymbol{C'_1}$ y $\boldsymbol{C'_2}$ are the fuzzy sets obtained from rules one and two, Fig. 6 shows a graphic illustration of the fuzzy system with several rules and several antecedents.

E. Defuzzification

The fuzzy system output may be comprised of several numerical values, as in this case, but sometimes, as well as in this case, the control system requires a single numerical value, which is f_e in this case, there are several ways of extracting a single numerical value from a fussy system output comprised by several values, among those methods, the centroid was used, based on equation (24).

$$Centroid_z = \frac{\int \mu_A(z) z dz}{\int \mu_A(z) dz}. \quad (24)$$

The variable μ_A is the system output. A decision surface is shown in Fig. 7 in which all possible input combinations are evaluated to show how the output would be.

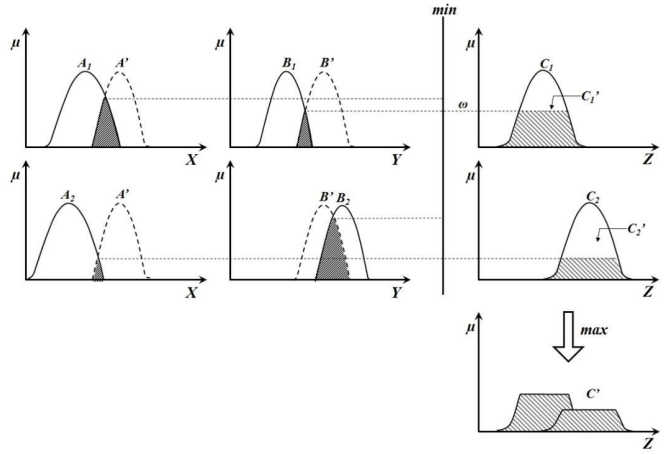

Fig. 6. Fuzzy system with several rules and several antecedents.

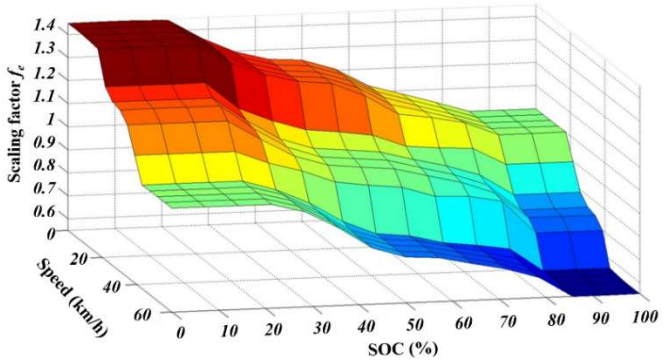

Fig. 7. Output (decision) surface of *FIS* for input combinations.

I. Results from the experiment

The proposed *EAS* was applied to a laboratory experimental test bench, which is shown in Fig. 8. Table 1 shows all parameters of the emulated *HEV*. The ultra-capacitor voltage has been limited to a safe maximum voltage lower than its real maximum limit. The driving path chosen for the experimental test is *ECE-15,* an urban cycle path, usually used for utilitarian vehicles test.

Initially, the system has a ran test without the proposed *EAS*. Fig. 9 shows the results of this initial test, Fig. 9(b) shows the *ECE-15* cycle, which maximum velocity is *50km/h;* the test was repeated *five* times. Fig. 9(a) shows the power send by the ultra-capacitor; the peak power delivered from the ultra-capacitor is near *7kW,* the maximum recharging power is around *3kW*. Fig. 9(c) shows the ultra-capacitor *SOC*; the *SOC* reaches values over 100%. When this happens, the dynamic braking (power resistors) dissipate the exceeding energy.

The same test (same parameters) was done with the proposed *EAS*. The results are shown in Fig. 10. Ultra-capacitors are

required to deliver more energy, which leads to deeper discharge, maintaining a larger availability to receive the charge from the regenerative braking. Fig. 10(s) shows the ultra-capacitor *SOC*, which reaches lower values compared to the former case. The capacitor *SOC* is limited by the DC-bus minimum voltage.

Table. 1 Parameters used for the test.

Parameter	Value
HE Vehicle	
Weight of the *HVE (kg)*	*1000*
Aerodynamic coefficient	*0.5*
Drag coefficient	$14x10^{-3}$
Area of the front (m^2)	*3.225*
The radius of tires *(m)*	*0.3*
Maximum velocity *(km/h)*	*50*
Maximum acceleration (m/s^2)	*0.7*
Fuel Cell Emulator (programable DC source)	
Nominal power *(W)*	*3000*
Nominal voltage *(V)*	*100*
Maximum current *(A)*	*30*
Battery	
Capacity *(Wh)*	*4000*
Nominal voltage *(V)*	*100*
Maximum discharge current *(A)*	*150*
Maximum charge current *(A)*	*75*
Ultra-Capacitor	
Capacity *(Wh)*	*112*
Maximum voltage *(V)*	*96*
Voltage limit *(V)*	*80*
Usable energy *(Wh)*	*100*
Maximum discharge current *(A)*	*1000*
Maximum charge current *(A)*	*1000*

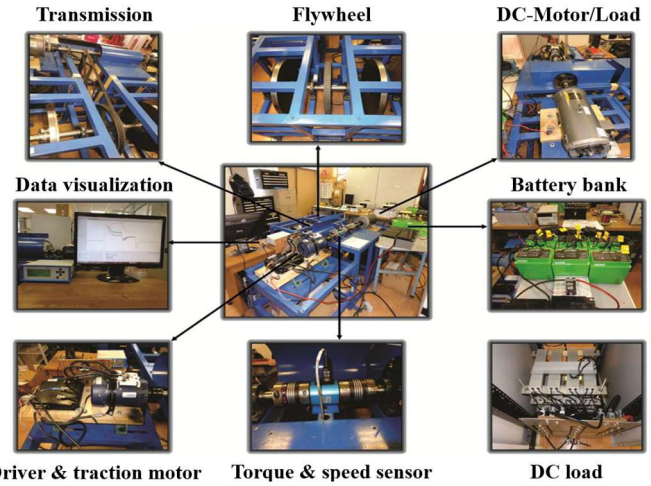

Fig. 8. Experimental testbed.

Finally, Fig. 11 shows the energy burned by the dynamic brake (resistive load) for both operations modes. The energy savings in the experiment is around *160* Wh; this is *14%* of the total energy used in the test. The proposed *EAS* for the 6 km test was *1.15 kWh*, in contrast to the *1.31 kWh*, used without the proposed *EAS*. The energy consumption by km is *192 Wh/km* with the proposed *EAS* against *218 Wh/km* without the proposed *EAS*. This produces the vehicle to drive *109* miles per gallon *mpg* with the proposed *EAS* against *96 mpg* without the proposed strategy.

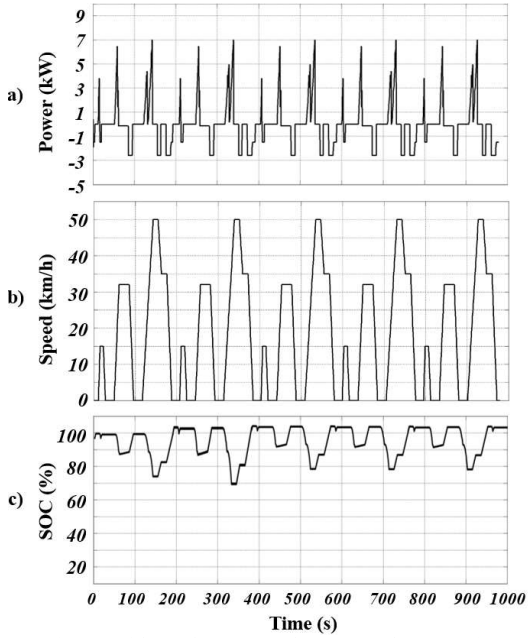

Fig. 9. Experiment without the proposed *EAS*: a) ultra-capacitors power, b) *ECE-15* drive cycle (5 cycles), c) ultra-capacitors *SOC*.

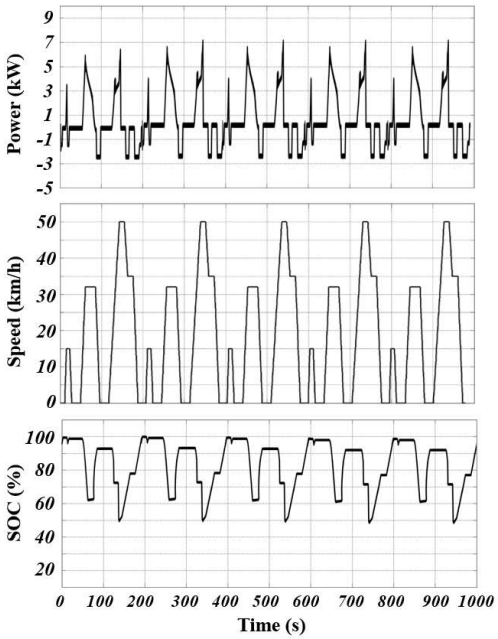

Fig. 10. Experiment with the proposed *EAS*: a) ultra-capacitors power, b) *ECE-15* drive cycle (5 cycles), c) ultra-capacitors SOC.

IV. Acknowledgment

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V. Conclusions

This article proposed a new Energy Administration Strategy *EAS* for a Hybrid Electric Vehicle *HEV,* which power systems

is composed of a fuel cell, a battery, and an ultra-capacitor. The strategy is based on the fuzzy logic approach. The proposed *EAS* was able to control the ultra-capacitor state of charge and take advantage of its superior energy storage capability. Experimental results showed that the proposed strategy reduced the waste of energy, which in other conditions would be burned in the dynamic brake, and at the same time, it satisfies the acceleration requirements imposed by the drive cycle *ECE-15*. Results show an energy saving of *160Wh* in the *6km* drive cycle test. The energy consumption decreased from *218 Wh/km* without the proposed *EAS* to *192 Wh/km*. The estimated fuel efficiency also increased from *96mpge* to *109mpge*.

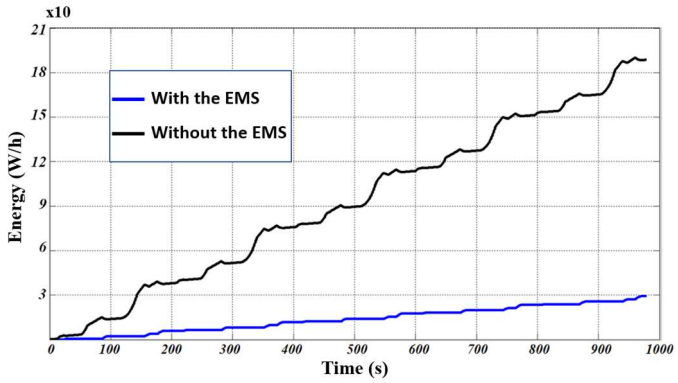

Fig. 11. The energy dissipated by the dynamic brake.

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Chapter 7

Energy-based Stabilizing Controllers for DC-DC Converters Feeding Constant Power Loads

Summary of the chapter

In this chapter an article intended to study the instability problem caused by the interconnection of DC converters with constant power loads (CPLs)is presented. A linear and a nonlinear energy-based approaches are proposed. Without the presence of CPLs, the stability of the DC-DC power converter is intrinsic, while with CPLs the stability must be induced, a task that is not easy with traditional control approaches. This paper shows that the stabilization of the power converter can be achieved in pure physical terms, using power and energy as the primary objectives, which can be done in a linear and a nonlinear approach. Also, considering the energy as the perspective for the problem provides a physical explanation to the stability issues, furthermore, it provides a clear practical solution, because now it is possible to link the parameters of the controller to nominal specifications that are used for power converter design. In this way, the strategies based on the power and energy are now based on known approaches, which is a difference to known approaches, whose stability are based on frequency domain, eigenvalue and immittance criteria. Experimental results are presented to corroborate the theoretical analysis.

Energy-based Stabilizing Controllers for DC-DC Converters Feeding Constant Power Loads

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***Abstract*—In this paper is studied and presented the solution for the instability problem caused by the interconnection of DC converters with constant power loads (CPLs). A linear and a nonlinear energy-based approaches are proposed. Without the presence of CPLs, the stability of the DC-DC power converter is intrinsic, while with CPLs the stability must be induced, a task that is not easy with traditional control approaches. This paper shows that the stabilization of the power converter can be achieved in pure physical terms, using power and energy as the primary objectives, which can be done in a linear and a nonlinear approach. Also, considering the energy as the perspective for the problem provides a physical explanation to the stability issues, furthermore, it provides a clear practical solution, because now it is possible to link the parameters of the controller to nominal specifications that are used for power converter design. In this way, the strategies based on the power and energy are now based on known approaches, which is a difference to known approaches, whose stability are based on frequency domain, eigenvalue and immittance criteria. Experimental results are presented to corroborate the theoretical analysis.**

***Index Terms*—DC-DC converters, constant power loads, stability.**

I. Introduction

The design and testing of switching DC converters are done in *stand-alone* operation with a passive (resistive) loads. Result of this, is their unpredictable response during their interconnection with active devices that prevents DC-DC converters to achieve an equilibrium. In particular, instability problems have been identified in the context of DC buses [1], due to the *negative impedance* characteristics of regulated devices, i.e. while the rate of change of voltage with respect to current in passive loads is positive, in the case of a regulated device, it is negative. This behaviour is characteristic of a case of instability generated by power converters acting as *constant power loads* (CPLs) [2]–[5].

Several studies on DC bus stablity are available, [6]–[8]. Nevertheless, after an extensive number of contributions on the DC bus stability topic, it is still a topic for study due that there are no a universal solution yet, existent contributions in [6]–[9] demonstrate for stability purposes only the condition of *sufficiency*. Stability margins are also frequently revised in [1], [10]. Some solutions have an impact in efficiency and power density. Since they involve the use of passive components to achieve stability [11], [12]. Another disadvantage of current solutions is that some require additional hardware. For example, the use of auxiliary shunt circuits to induce stability on the DC bus in [9], [13], [14], involving additional costs. Some solutions require energy storage systems. This is a very plausible and practical solution in modern scenarios [14]–[18], though these components are not always available in DC networks for these particular purposes. Stabilizing controllers can be in conflict with other control objectives. Stabilization via controller design for source converters might score low in modularity, i.e. the lack of freedom in controller selection yields a risk of conflict with maximum power point tracking, optimal control and the hierarchical control of smart/micro grids in [6], [19], which potentially limits their application.

Feedback control for stabilization is the main study of this paper, by endowing stabilization properties to controllers, this paper proposes a set of controllers to induce bus voltage stability, which are validated theoretically and experimentally. Motivated by the increased interest in the development of DC network interfaces for renewable energy integration, (on-board, grid connected and islanded) micro grids, modern energy distribution networks, etc.

The current stability conditions for DC grids propose different stabilization strategies based on abstract mathematical domains e.g. frequency domain criteria, Lyapunov approaches, eigenvalue- and impedance or admittance characteristics- analyses [13]–[18], however they do not propose an explanation to the physical problem, the unstable performance of power converters is the result of the power imbalance generated by non-passive loads, so, stabilization is the mechanism to induce a balance. The proposed solutions are based on a physical parametrization of the converter such as energy, power and nominal operation, since they are important parameters for power converter design. Thus, stabillity can be prognosticated by the user based on the energy and power specifications, which is not an easy task where stability is purely associated to other abstract mathematical domains.

Theoretical analysis for the development of the stabilizing linear and nonlinear energy controllers are validated by experiments.

II. System modeling and Notation

This paper notation is as follows, (A, B) are used to represent matrices in which the A is obtained by stacking it over B; I_m is the identity matrix with the number of rows and columns equal to m; $0_{p\times q}$ is used to express a matrix of zeros with p rows and q columns; and the matrix $A^\top$ is used to express the transpose matrix.

In this paper, to represent a proper procedure for the results of the controller, the modeling specification is as follows:

$$D_0 u + \cdots + D_L \frac{d^L}{dt^L} u = P_0 w + \cdots + P_N \frac{d^N}{dt^N} w, \quad (1)$$

where $D_i \in \mathbb{R}^{p\times q}$, $i = 0, ..., L$, and $P_j \in \mathbb{R}^{p\times g}$, $j = 0, ..., N$, $u := (u_1, u_2, \ldots, u_q)$ are *external variables* and $w := (w_1, w_2, \ldots, w_g)$ are latent variables; This group of equations can be accommodate as

$$D\left(\frac{d}{dt}\right) u = H\left(\frac{d}{dt}\right) w \; ; \quad (2)$$

where $D\left(\frac{d}{dt}\right)$ is a polynomial matrix with dimension $p\times(L+1)q$ and $H\left(\frac{d}{dt}\right)$ is a matrix with dimension $p\times(N+1)g$. If $D\left(\frac{d}{dt}\right)$ is a full row rank or a singular matrix, then

$$u = \underbrace{P\left(\frac{d}{dt}\right)}_{D\left(\frac{d}{dt}\right)^* H\left(\frac{d}{dt}\right)} w \; ; \quad (3)$$

where $D\left(\frac{d}{dt}\right)^*$ is the left inverse of it $D\left(\frac{d}{dt}\right)$. If the system is controllable, then the equation (3) can be obtained, it is "called image representation" [20]. In this representation the system can be divided in inputs and outputs, as follows

$$\underbrace{\begin{bmatrix} o \\ y \end{bmatrix}}_{=u} = \underbrace{\begin{bmatrix} O\left(\frac{d}{dt}\right) \\ Y\left(\frac{d}{dt}\right) \end{bmatrix}}_{=P\left(\frac{d}{dt}\right)} w \; ; \quad (4)$$

where w and o have the same number of components. Note that (4) is similar to the concept of the transfer function $(Y(s)O(s)^{-1})$.

Applying this concepts to our purpose, it is possible to model power converters with input and outputs with the same number of variables, whose product is equal to the power of the converter.

III. Analysis in terms of energy

By considering the image representation it is possible to describe the dynamics of power converters in terms of power and energy. This can be achieved via the input-output separation, $u = (V, I)$, where, with the same number m of components, V and I denote the voltage and current vectors, respectively. In this way, the input power will be

$$Q_p(u) := \frac{1}{2} u^\top \begin{bmatrix} 0 & I_m \\ I_m & 0 \end{bmatrix} u = V^\top I \; .$$

Considering (3), it is possible to obtain the following

$$Q_p(u) = Q_p(w) := \frac{1}{2}\left(P\left(\frac{d}{dt}\right) w\right)^\top \begin{bmatrix} 0 & I_m \\ I_m & 0 \end{bmatrix} P\left(\frac{d}{dt}\right) w \; . \quad (5)$$

Where Q_p is the supply rate.

A. Passive systems

Passive circuits which are linear systems, can not have a transfer function with elements in the right half plane, otherwise it would be unstable, which means that variables as voltages and currents are able to increase without limit even without a power source. Passive systems are input-output stables ([21]). This means that for a bounded input they always provide a bounded-output.

Energy storage in passive circuits is denoted by Q_E, which can not be greater than the input power denoted by Q_p, this can be expressed as

$$Q_p \geq \frac{d}{dt} Q_E \quad (6)$$

Where the energy storage must be greater than zero, i.e. $Q_E \geq 0$.

From (6) it is easy to conclude that the portion of the energy has been dissipated, and the other has been stored. This dissipated energy is denoted as Q_d, then the following expression is valid

$$Q_p = \frac{d}{dt} Q_E + Q_d \; . \quad (7)$$

where, for example, the energy that has been dissipated is the result of a resistor in a passive circuit.

B. Energy-based linear stabilization

Instability usually manifest in the form of voltage oscillations, mainly in DC buses. The main study of this paper is on CPL producing this effect and how to avoid it by *power balancing*, but first it is convenient to describe the DC bus in the form of some equations underlying its capacitor

$$C\frac{d}{dt} v = i_{in} - i_{out} \; ; \quad (8)$$

where v is the DC bus voltage, i_{in} is the input current to the bus and i_{out} is the output current of the bus. A consequence of (8), is that the voltage is constant if the right side of the equation has no change, which means that

$$i_{in} = i_{out} \; , \quad (9)$$

equation (9) express an equilibrium achieved in steady state. An expression for the power of the DC bus is easily achieved just by multiplying (8) by the voltage v as follows

$$vC\frac{d}{dt} v = \frac{1}{2} C \frac{d}{dt} v^2 = v i_{in} - v i_{out} \; ; \quad (10)$$

If the bus is feeding a passive element, such as a resistor, then the output current will be $i_{out} = \frac{v}{R}$, as previously mentioned, this case is an enough condition for passivity and

for input-output stability. From (7) it can be noticed that $Q_E = \frac{1}{2}Cv^2 \geq 0$, $Q_p = vi_{in}$ and $Q_d = vi_{out} = \frac{v^2}{R} \geq 0$.

Even when the previous condition is ideal to an input-output stability, if a CPL is present in the circuit, then $vi_{out} \geq 0$ is not a dissipation function, because it is not been satisfied at any time, as in the case of $\frac{v^2}{R} \geq 0$. Stable operation of a power converter is easy to ensure without interacting with a CPL, but in a network operation, where CPLs or another elements are presents, this stability is not always guaranteed.

If the power delivered to the CPL is denoted by Q_{CPL}, it is possible to express (8) as

$$\underbrace{vi_{in}}_{Q_P} = \underbrace{\frac{1}{2}C\frac{d}{dt}v^2}_{\frac{d}{dt}Q_E} + \underbrace{vi_{out}}_{Q_{\text{CPL}}} ,$$

The interconnection of the power converter with the CPL can be induced by adding an additional term, this term is the dissipation, such that (7) is satisfied, resulting in

$$Q_p - \frac{d}{dt}Q_E - Q_{CPL} = Q_d \geq 0 \, . \tag{11}$$

From (11), it is possible to conclude that it is possible to induce stability in power converters by adding the additional term, then it can read as: *"if the dissipation is greater than the power delivered to the CPL, stability is achieved"*.

C. Energy-based stabilization via LMIs

A method to achieve stability is presented in this section, based on *linear matrix inequalities* (LMIs). In order to do so, note first that since

$$Pw = P_0 w + P_1 \frac{d}{dt}w + ... + P_N \frac{d^N}{dt^N}w \, , \tag{12}$$

where P_i, $i = 0, ..., N$ are $q \times m$ block matrices of coefficients. It is possible to factorize as

$$Pw = \begin{bmatrix} P_0 & P_1 & \cdots & P_N \end{bmatrix} \begin{bmatrix} w \\ \frac{d}{dt}w \\ \vdots \\ \frac{d^N}{dt^N}w \end{bmatrix} .$$

Matrix of coefficients $q \times (N+1)m$ is defined as

$$\widetilde{P} := \begin{bmatrix} P_0 & P_1 & \cdots & P_N \end{bmatrix} . \tag{13}$$

The following factorization of the energy function is possible due to the general principle that every system in which the supply, is a power rate, energy is in function of state variables. According to this, the following is obtained

$$Q_E(w) = \begin{bmatrix} w^\top & \frac{d}{dt}w^\top & \cdots & \frac{d^{N-1}}{dt^{N-1}}w^\top \end{bmatrix} K \begin{bmatrix} w \\ \frac{d}{dt}w \\ \vdots \\ \frac{d^{N-1}}{dt^{N-1}}w \end{bmatrix} , \tag{14}$$

where $K = K^\top \geq 0$ is an $Nm \times Nm$ constant matrix. By considering (14) and defining

$$u^\top := \begin{bmatrix} w^\top & \frac{d}{dt}w^\top & \cdots & \frac{d^{L-1}}{dt^{L-1}}w^\top \end{bmatrix} ,$$

it is possible to obtained the derivative of the energy

$$\frac{d}{dt}E(w) = \frac{d}{dt}\left(v^\top K v\right) = \frac{d}{dt}v^\top K v + v^\top K \frac{d}{dt}v \, .$$

Consequently, we can express (11) as

$$\begin{aligned} &\overbrace{\frac{1}{2}v^\top \widetilde{P}^\top \begin{bmatrix} 0_{m\times m} & I_m \\ I_m & 0_{m\times m} \end{bmatrix} \widetilde{P}v}^{Q_p} \\ &\underbrace{-v^\top \begin{bmatrix} 0_{m\times Lm} & 0_{m\times m} \\ K & 0_{Lm\times m} \end{bmatrix} v - v^\top \begin{bmatrix} 0_{Lm\times m} & K \\ 0_{m\times m} & 0_{m\times Lm} \end{bmatrix} v}_{-\frac{d}{dt}E} \\ &\underbrace{-v^\top \widetilde{R} v}_{-Q_{CPL}} \geq 0 \, ; \end{aligned} \tag{15}$$

where $Q_D \geq 0$ is achieved by establishing "≥ 0" which is a consequence of the dissipation condition, and Q_{CPL} is the power extracted by the CPL as a linear approximation in the form of a constant matrix $\widetilde{R}$ and the latent variable w.

It is possible to reduce (15) to just find a matrix $K = K^\top \geq 0$ that satisfies the following expression

$$\begin{aligned} &\frac{1}{2}\widetilde{P}^\top \begin{bmatrix} 0_{m\times m} & I_m \\ I_m & 0_{m\times m} \end{bmatrix} \widetilde{P} - \begin{bmatrix} 0_{m\times Nm} & 0_{m\times m} \\ K & 0_{Nm\times m} \end{bmatrix} \\ &- \begin{bmatrix} 0_{Nm\times m} & K \\ 0_{m\times m} & 0_{m\times Nm} \end{bmatrix} - \widetilde{R} \geq 0 \, ; \end{aligned} \tag{16}$$

which is the energy stabilization condition, an expression that can be obtained by standard LMI solvers as the Yalmip toolbox of Matlab.

IV. Power-based linear control design

In this section the control designed is developed. For this purpose, a boost converter feeding a CPL will be considered as is shown in Fig. 1. This selection is made due that it is an interconnection potentially unstable.

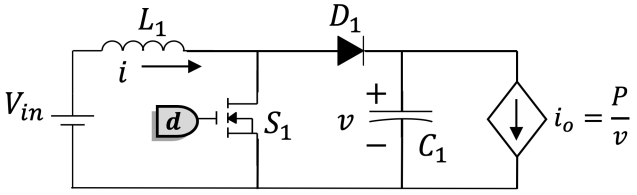

Fig. 1. Boost converter feeding a CPL.

The equations of the converter are

$$\begin{aligned} L\frac{d}{dt}i &= -(1-d)v + V_{in} \\ C\frac{d}{dt}v &= (1-d)i - i_o \end{aligned} \tag{17}$$

where i is the current through the inductor and and v is the voltage of the capacitor C. V_{in} is the input voltage; d is the duty cycle; P is the output power of the boost converter; and i_o is the output current of the converter that flows through the CPL.

A. Small signal controller

In this section a small signal controller is proposed, according to equations (17). The notation used to describe the controller is as follows, incremental variables are designed by $\Delta x := x - \overline{x}$, where x is the original variable and $\overline{x}$ is the desired equilibrium point. If (17) is expressed according to that small signal representation, the following is obtained

$$\begin{aligned} \overline{v} &= \frac{1}{(1-\overline{d})}\overline{V}_{in} \\ \bar{i} &= \frac{1}{(1-\overline{d})}\bar{i}_o \end{aligned} \tag{18}$$

Then the small signal model is obtained as

$$\begin{aligned} L\frac{d}{dt}\Delta i &= -(1-\overline{d})\Delta v + \overline{v}\Delta d + \Delta V_{in} \\ C\frac{d}{dt}\Delta v &= (1-\overline{d})\Delta i - \bar{i}\Delta d - \Delta i_o \end{aligned} \tag{19}$$

where $\Delta i_o = -\frac{P}{\overline{v}^2}\Delta v$.

In this section energy based controllers for the input current and the output voltage are used to induce stability, for this, they are defined next. For the current controller the control law is defined as

$$\Delta d := -k_1 x_1 - k_2 \Delta i \ ; \tag{22}$$

where x_1, is the result of the integral of the error, and k_1, k_2 are the controller gains. The equation of the integral, which tracks the reference r is given as follows

$$\frac{d}{dt}x = \Delta i - r \ . \tag{23}$$

The output voltage controller is defined as

$$r := -g_1 x_2 - g_2 \Delta v \ ; \tag{24}$$

where x_2, is the result of the integral of the error $\Delta v = v - \overline{v}$, which in the ideal case it must be zero, and g_1, g_2 are the controller gains. The equation of the integral, which tracks the reference $\Delta v =$ is given as follows

$$\frac{d}{dt}x_2 = \Delta v \ . \tag{25}$$

Using previous equations, the small signal model can be obtained in the form of (2), in which external variables are $u := (\Delta V_{in}, \Delta i_o, \Delta i, \Delta v)$ and the latent variable are $w := (x_1, x_2)$, the result is as follows

$$D := \begin{bmatrix} 1 & 0 & -L\frac{d}{dt} - k_2\overline{v} & -(1-\overline{d}) \\ 0 & 1 & -(1-\overline{d}) - k_2\bar{i} & C\frac{d}{dt} \\ 0 & 0 & 1 & g_2 \\ 0 & 0 & 0 & 1 \end{bmatrix} \ ; \tag{26}$$

$$H := \begin{bmatrix} k_1\overline{v} & 0 \\ k_1\bar{i} & 0 \\ \frac{d}{dt} & -g_1 \\ 0 & \frac{d}{dt} \end{bmatrix} \ . \tag{27}$$

The image representation of $P := D^{-1}H$, is shown in (20), and its coefficient matrix is shown in (21). The output power of the DC bus, which is the same the CPL consumes, is expresses as $\Delta i_o \Delta v = -\frac{P}{\overline{v}^2}\Delta v^2$, which can be written in terms of the latent variable using (25), i.e.

$$Q_{CPL}(z) = -\frac{P}{\overline{v}^2}\left(\frac{d}{dt}x_2\right)^2 \ ;$$

then the coefficient matrix $\widetilde{R}$ in (16) is given by

$$\widetilde{R} := \begin{bmatrix} 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & -\frac{P}{\overline{v}^2} & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 \end{bmatrix} \ . \tag{28}$$

The controllers for stabilization are form by obtaining the gains k_1, k_2, g_1, g_2 and obtaining K in (16). The control loop is shown in Fig. 2.

V. Nonlinear energy-based control design

This section describes a stabilization control scheme based on a energy storage analysis; this is a more suitable approach for the nonlinear case. In addition, the difficulties of non-linear control of DC converters feeding CPLs are presented. And thus, it is shown that it is possible to carry out these problems more easily with the help of scheme based on a energy storage analysis.

A. Design complications in classic current control

The non-minimum phase behavior of DC converters leads to stabilization by means of current control and, as a matter of fact, a voltage compensator loop is added which allows voltage regulation under input voltage variations [22]. This point of fact can be analyzed by means of (17).

To induce input current stabilization, the following duty cycle equation can be used

$$d := 1 - \frac{1}{v}\left[k(i-r) + V_{in}\right] \ ,$$

since

$$\frac{d}{dt}i = -\frac{k}{L}(i-r) \ ;$$

where k and r are a positive gain and the reference, respectively, and which can induce stability. In order to guarantee stability at the origin, *zero dynamics* definition is employed for validation, this condition establishes that a system is stable if any path of v has an input $d = 0$ and a initial condition $i(0) = 0$. Using the following equation, the trajectories can be generated

$$C\frac{d}{dt}v = -i_o \ ;$$

$$\begin{bmatrix}\Delta V_{in}\\ \Delta i_o\\ \Delta i\\ \Delta v\end{bmatrix} = \underbrace{\begin{bmatrix} k_1\overline{v}+k_2\overline{v}\frac{d}{dt}+L\frac{d^2}{dt^2} & -g_1k_2\overline{v}+(1-d-g_1L-g_2k_2\overline{v})\frac{d}{dt}-g_2L\frac{d^2}{dt^2}\\ \bar{i}k_1+(1-d+\bar{i}k_2)\frac{d}{dt} & g_1(d-1-\bar{i}k_2)+g_2(d-1-\bar{i}k_2)\frac{d}{dt}-C\frac{d^2}{dt^2}\\ \frac{d}{dt} & -g_1-g_2\frac{d}{dt}\\ 0 & \frac{d}{dt}\end{bmatrix}}_{P\left(\frac{d}{dt}\right)}\begin{bmatrix}x_1\\ x_2\end{bmatrix} . \tag{20}$$

$$\widetilde{P} := \begin{bmatrix} k_1\overline{v} & -g_1k_2\overline{v} & k_2\overline{v} & (1-d-g_1L-g_2k_2\overline{v}) & L & -g_2L\\ \bar{i}k_1 & g_1(d-1-\bar{i}k_2) & (1-d+\bar{i}k_2) & g_2(d-1-\bar{i}k_2) & 0 & -C\\ 0 & -g_1 & 1 & -g_2 & 0 & 0\\ 0 & 0 & 0 & 1 & 0 & 0\end{bmatrix} . \tag{21}$$

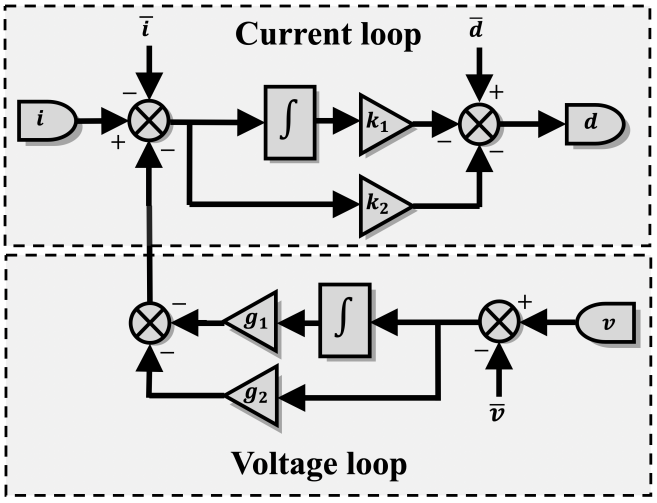

Fig. 2. Energy-based linear controller diagram.

this is satisfied when the converter operates in stand-alone mode with a resistive load, such that $i_o = \frac{v}{R}$. Nevertheless, when connecting a CPL as load is not satisfied, since its zero dynamics condition holds that

$$C\frac{d}{dt}v = -\frac{P}{v} ;$$

since discontinuity exists and has no solution to zero when v tends to zero.

B. Nonlinear controller for energy-based stabilization

To overcome the complication of designing controllers for output voltage and input current, we resort to a physical analysis based on the energy stored in the converter, this is represented by

$$Q_E = Q_L + Q_C ,$$

where $Q_L = \frac{1}{2}Li^2$ and $Q_C = \frac{1}{2}Cv^2$. Recall that the power flow in these converters is only in one direction, in other words, $i \geq 0$ an $v \geq 0$.

Then, performing a *nonlinear transformation* the *observable pairs* ((Q_L, i) and (Q_C, v)) are obtained, this implies any path of one is equal to a single path of the other. In this way, a single equilibrium point can be achieved and stabilization properties can be shared between them. Recall that the current and the voltage from the inductor and capacitor, respectively, describes the stored energy in the system and vice-versa.

If state variables are defined from energy equations, (17) and $i_o = -\frac{P}{v}$ can be transformed into

$$\begin{cases} \frac{d}{dt}Q_L = iL\frac{d}{dt}i = -(1-d)vi + V_{in}i \\ \frac{d}{dt}Q_C = vC\frac{d}{dt}v = (1-d)vi - P \end{cases} . \tag{29}$$

To induce stability, it is proposed the following controller based on the energy from the inductor

$$d := 1 - \frac{1}{vi}\left[k_1(Q_L - r) + V_{in}i\right] ,$$

what results in

$$\frac{d}{dt}Q_L = -k_1(Q_L - r) ;$$

where k_1 and r are the gain (positive) and the energy reference from the inductor, respectively. As in the previous case, it is also used the *zero dynamics* definition to verify stability.

$$\frac{d}{dt}Q_C = -P ;$$

which guarantees stabilization at the origin, due to P(must be positive). By setting r as the input current reference, output voltage stabilization can be achieved

$$r := -k_2x ,$$

where k_2 and x are a gain and the solution of capacitor energy, respectively, notice that the reference is defined by the chosen output voltage equilibrium point $\overline{v}$, i.e.

$$\frac{d}{dt}x = \frac{1}{2}C(v^2 - \overline{v}^2) .$$

Fig. 3 depicts the the developed controller. This control approach is able to guarantee stabilization of voltage bus when power converters feeds a CPL. Both control approaches were designed in terms of power and energy, the advantage of linear control lies in its ease of implementation due to the linearity of its structure, while non-linear control can be optimized in the large signal space.

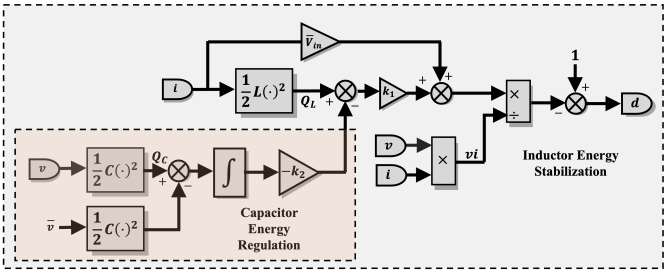

Fig. 3. Energy-based nonlinear controller diagram.

VI. Experimental results

This section presents the experiments needed to corroborate the controller design presented for both linear and non-linear cases. The experiments were performed using two boost converters, one operating as a source and the other as a CPL. The control algorithm for both cases were tested using DSP TI28335 with a sampling frequency of 100 kHz to acquire the voltage and current signals. The signals for the Mosfet gate are at 50 kHz. The converter operating as CPL feeds an electronic load BK8616. The information related to the experiments is shown in Table I. As aforementioned, the constant power load operates using a boost converter and a discrete-time controller is implemented running at 50kHz, the gains for this controller are $k_1 = 0.033$ and $k_2 := 0.043$. Fig. 4 illustrates the diagram of the experimental hardware setup. Experiments for both controllers are presented in the following subsections in more detail.

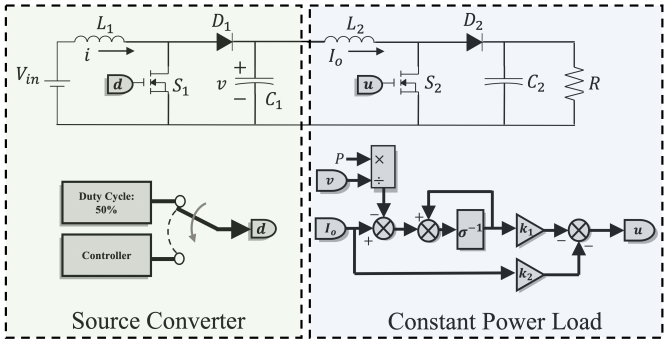

Fig. 4. Controller diagram used in the experimental setup.

A. Experimental results for the energy-based linear controller

Fig. 2 shows the linear controller implemented in this test, the gains of this controller were calculated by the solution of (16) with the help of `Yalmip` toolbox, which resulted in the following gains $k_1 := 0.0213$, $k_2 := 0.0804$, $g_1 := 7.0221$, $g_2 := 5.7691$. The first experiment starts with an open loop test with a continuous duty cycle of $d := 0.5$, with this configuration, the oscillatory behavior of the system can be observed, after a certain time, the proposed linear controller is activated where stabilization can be observed. The behavior of the system in this experiment can be seen in Fig. 5.

TABLE I
Implementation parameters

Parameter	*Description*	*Value/Part*
V_{in}	*Converter nominal input voltage*	$50V$
V_{C1}	*Converter nominal output voltage*	$100V$
L_1, L_2	*Inductors 1 and 2*	$240\mu H$
C_1, C_2	*Capacitors 1 and 2*	$10\mu F$
S_1, S_2	*MOSFETs 1 and 2*	*IRFP264pbf*
D_1, D_2	*Diodes 1 and 2*	*MBR40250G*
R	*Resistor (Electronic load)*	150Ω
f_s	*Sampling frequency (controller)*	$100kHz$
f_c	*Switching Frequency*	$50kHz$
P	*Nominal power of CPL*	$200W$

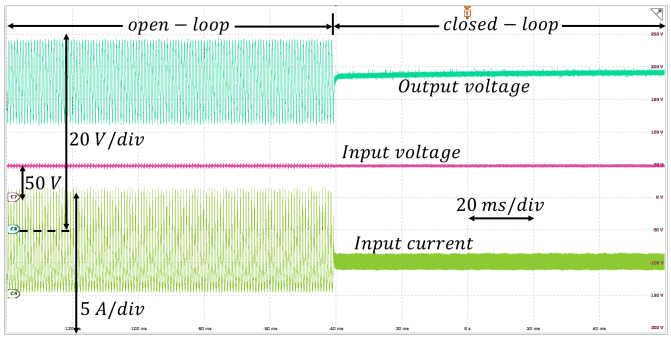

Fig. 5. Experimental results of the energy-based linear controller activated at a certain time.

B. Experimental results for the energy-based nonlinear controller

This subsection describes experiment carried out to show the behavior of the proposed nonlinear control scheme, the controller implemented is illustrated in Fig. 3. The computed gains from the corresponding analysis are $k_1 := 50000$ and $k_2 := 800$.

As in the previous case, this experiment starts with an open loop test with a continuous duty cycle of $d := 0.5$, the oscillatory behavior of the system can be observed, and after a certain time, the proposed nonlinear controller is activated where stabilization can be observed. The behavior of the system in this experiment can be seen in Fig. 6.

VII. Conclusions

In this work, two novel control approaches were developed to deal with the stabilization problems generated by the interconnection of power converters with CPLs. The proposed control schemes are based on the physical design parameters (power and energy) of the converter. This fact, gives the user the possibility to predict and interpret the stability margins of the system by means of physical (energy and power) specifications. The experimental tests show the stabilization benefits of both controllers.

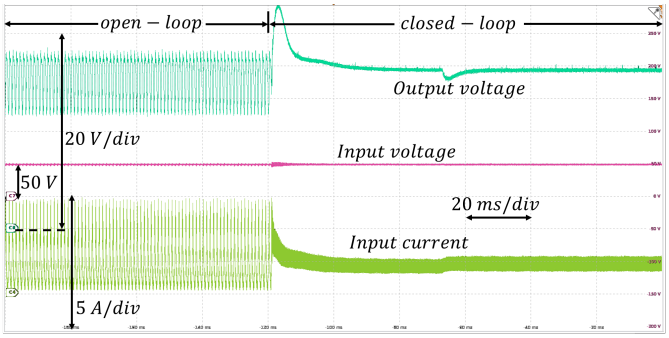

Fig. 6. Experimental results of the energy-based nonlinear controller activated at a certain time.

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Chapter 8

Modeling and Control of an Interleaved DC-DC Multilevel Boost Converter

Summary of the chapter

In this chapter, an article to study the modeling and control of an interleaved DC-DC multilevel topology that exhibits a high-voltage gain and a minimum ripple point design. In this configuration, the current ripple cancelation point can be arbitrarily defined according to a desired specification, which represents an advantage with respect to classical topologies whose minimum ripple point is constrained (e.g. by a duty cycle equal to 0.5). We present a generalized model for the converter that is valid for any number of levels and useful for control purposes. Experimental results of the ripple cancelation as well as a closed-loop implementation is presented.

Modeling and Control of an Interleaved DC-DC Multilevel Boost Converter

C.A. Villarreal-Hernandez, J.C. Mayo-Maldonado, J.E. Valdez-Resendiz, J.C. Rosas-Caro

***Abstract*—In this paper we study the modeling and control of an interleaved DC-DC multilevel topology that exhibits a high-voltage gain and a minimum ripple point design. In this configuration, the current ripple cancelation point can be arbitrarily defined according to a desired specification, which represents an advantage with respect to classical topologies whose minimum ripple point is constrained (e.g. by a duty cycle equal to 0.5). We present a generalized model for the converter that is valid for any number of levels and useful for control purposes. Experimental results of the ripple cancelation as well as a closed-loop implementation is presented.**

Keywords—Current ripple cancelation; dc/dc converters; multilevel converters, switched capacitors.

I. INTRODUCTION

The inclusion of renewable energy generation in electric distribution systems has been significantly increasing in the last years. In particular, renewable sources such as solar panels are getting increased attention due to their continuously decreasing prices. However, this kind of energy has some features that complicate its exploitation, such as low voltage of generation and intermittence. Moreover, it is well known that the discontinuous nature of the input current ripple of converters that are connected to photovoltaic panels, affects the efficiency and lifetime (see [1]) of the cells, consequently the implementation of converters with ripple cancelation characteristics is highly desirable.

Several DC-DC converters topologies presenting voltage step-up solutions have been proposed in literature, for this purpose transformers and coupled inductors are a common solution, in [2] a coupled inductor boost topology is proposed to have a high output voltage, similarly in [3] is presented a ripple passive filter using coupled inductors, nevertheless coupled inductors and transformers represent an increase in weight and size of the converter. This is why topologies without coupled inductors are desirable, for instance, in [4], is presented a topology which has an high gain compared to a regular boost topology, also provides a ripple free input current, but such topology has a fixed operation point, in such a way that a duty cycle can only adopt a nominal value equal to 0.5. Another topology with high voltage gain is presented in [5], where a multilevel topology is proposed without the use of transformers or extreme duty cycles, also, this topology has no restriction in the number of step-up voltage levels, nevertheless the input current ripple is still present in this topology. An improvement to this multilevel topology is presented in [6], where an inductor is added to the topology in order to have a resonant switching which improves the efficiency of the converter, however, the input current has no ripple cancelation.

The interleaved multilevel boost converter studied in this paper offers compelling features for applications such as renewable energy systems, e.g. characteristics such as high input-to-output voltage gain, input-current ripple mitigation, small-size components due to its multilevel structure, a modular structure that facilitate further upgrades in voltage gains, etc. (cf. [7]- [8]). Although this is a switched capacitor converter that enables such compelling features, its modeling and control is not a straightforward matter. For instance, it is well-known that the traditional *state averaging* technique is not applicable in topologies with switched capacitors (see [9],[10]). Moreover, the advantage of a modular structure of the converter yields a major challenge to its analysis since the complexity of the dynamic model increases when new stages are connected, which corresponds to mathematical descriptions with an excessive number of variables and equations.

The issue of dynamic modeling and control using a large signal dynamic model based on instantaneous values of a multilevel boost converter and an early approach of a reduced order dynamic model of this converter for control purposes has been studied in [11]. A novel averaging approach to the modeling of the multilevel boost converter has been reported in [12], where a plausible nonlinear framework that considers the average losses of the converter is proposed. Nevertheless, the development of nonlinear control techniques to deal with the resulting highly nonlinear structure is still an open problem. Naturally, the complexity of the converter increases when we consider an interleaved version of this converter.

Prompted by these issues we propose a generalized model to deal with its underlying switched capacitor structure exhibiting the lowest possible dynamical complexity, even for the interleaved version of the converter, that is suitable for control purposes either in a linear or nonlinear setting. The proposed analysis is validated in closed-loop operation under typical disturbances.

II. MODELING OF THE INTERLEAVED TOPOLOGY

In this section, we employ a *reduced-order* approach (cf. [9]) to obtain approximate average dynamic model of two topologies, a *multilevel boost converter* (see [8]) in Fig. 1 a) and a *single-inductor multiplier Cuk converter* (see [13]) in Fig. 1 b). Then we combine both models with a *minimum ripple point* design in order to develop the model of the underlying interleaved topology (see e.g. Fig. 1 c)).

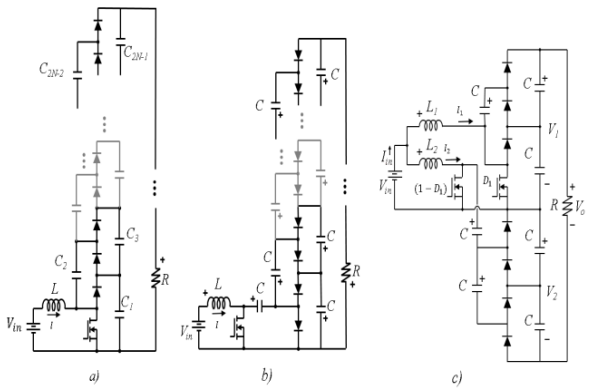

Fig. 1. a) Nx Multilevel boost converter; b) Nx Single-inductor Multiplier Converter; c) 4x Interleaved Multilevel Boost Converter

A. Multilevel Boost Converter

We now introduce a generalized model for this topology, i.e. a model for an arbitrary number multiplier stages and capacitors, using a reduced number of variables and equations. In other words, we show that although the *multilevel boost converter* can have a fixed but otherwise arbitrary number *N* of output capacitors, the complexity of its dynamic equations is analogous with respect to that of the basic *boost converter* which has only one capacitor.

The electric diagram of an *Nx* multilevel boost converter is shown in Fig. 1 a). In order to emphasize the motivation of a reduced-order model and as a preamble for the derivation of such model, we first consider a state-space averaging modeling approach that has been developed for switched-capacitor converters in [12]. By inspecting the equivalent circuits when the switch is open and closed in Fig. 1 a), we can obtain the following dynamic model.

$$
\begin{aligned}
L\frac{di}{dt} &= V_{in} - (1-D)V_1 \\
C_1\frac{d}{dt}V_1 &= (1-D)I - \frac{V_1 - V_2}{R_{eq1}} - \sum_{k=1}^{N}\frac{1}{R}V_{2k-1}\,, \\
C_2\frac{d}{dt}V_2 &= \frac{V_1 - V_2}{R_{eq1}} - \frac{V_2 - V_3}{R_{eq2}}, \\
C_3\frac{d}{dt}V_3 &= \frac{V_2 - V_3}{R_{eq2}} - \frac{V_3 - V_4}{R_{eq3}} - \sum_{k=1}^{N}\frac{1}{R}V_{2k-1}\,, \\
&\vdots \\
C_{2N-2}\frac{d}{dt}V_{2N-2} &= \frac{V_{2N-3} - V_{2N-2}}{R_{eq_{N-2}}} - \frac{V_{2N-2} - V_{2N-1}}{R_{eq_{N-1}}}, \\
C_{2N-1}\frac{d}{dt}V_{2N-1} &= \frac{V_{2N-2} - V_{2N-1}}{R_{eq_{N-1}}} - \sum_{k=1}^{N}\frac{1}{R}V_{2k-1}\,,
\end{aligned}
\qquad (1)
$$

where *N* corresponds to the number of capacitors at the output of the converter, and the expressions involving the parameters R_{eq_i} are accounted for the average energy losses of the converter due to the energy transfer between parallel capacitors over a switching period (cf. [12]). Note that while the main advantage of the multilevel boost converter is its high input-to-output voltage gain, which can be increased by adding switched capacitor levels at the output, there is a major problem in adding stages, since each switched capacitor level implies the addition of three dynamic equations to its model. For this reason, the derivation of a reduced order model results of central importance.

In the following, for the simplicity of exposition we assume that the value of the capacitors of the converter have the same value *C*, moreover we define the output voltage of the *Nx* multiplier boost converter as

$$
V_o = \sum_{k=1}^{N} V_{2k-1} \approx NV_i\,, \qquad (2)
$$

with $i = 1, \dots, N$, corresponding to the sum of the voltages across the capacitors at the output, which are approximated to have the same average value due to their voltage balancing property (see [9]). Consequently, by substituting the following relationships

$$
V_i = V_j, \qquad (3)
$$

and

$$
V_o = NV_i, \qquad (4)
$$

with $i, j = 1, \dots, 2N-1$, in (1) we obtain a reduced order set of dynamic equations.

$$
\begin{aligned}
L\frac{di}{dt} &= V_{in} - \frac{(1-D)}{N}V_o\,, \\
\left(\frac{2N-1}{N}\right)C\frac{d}{dt}V_o &= (1-D)I - N\frac{V_o}{R}\,,
\end{aligned}
\qquad (5)
$$

Note that the complexity of the model in (5) is the same as the one of the traditional boost converter. Moreover, it can also be noticed that the traditional average model of the boost converter is a special case of the one in (5) when we consider only one level, i.e. *N=1*.

B. Single Inductor Multiplier Cuk Converter

We now introduce a model for a single-inductor multiplier Cuk converter which is depicted in Fig. 1 b). For simplicity of exposition we assume that every capacitor has a value *C*. Consequently, using the same rationale as in the previous section, we obtain the following reduced-order model.

$$L\frac{d}{dt}I = V_{in} - \frac{(1-D)V_o}{N},$$
$$NC\frac{d}{dt}V_o = (1-D)I - \frac{N}{R}(V_o); \quad (6)$$

C. Interleaved Multilevel Boost Converter

The main idea of interleaving the previously studied converters is to achieve a total input current ripple cancellation. When interconnecting the converters in an interleaved way, the model of the overall topology can be easily obtained as shown in (7). For simplicity of exposition, we assume that both converters have the same number N of stages, corresponding to a total gain of $2N$ the input voltage.

$$\begin{gathered} L_1\frac{d}{dt}I_1 = V_{in} - \frac{(1-D_1)}{N}V_1 \\ \left(\frac{2N-1}{N}\right)C\frac{d}{dt}V_1 = (1-D_1)I_1 - \frac{N}{R}(V_1+V_2) \\ L_2\frac{d}{dt}I_2 = V_{in} - \frac{(1-D_2)}{N}(V_1+V_2) \\ NC\frac{d}{dt}V_2 = (1-D_2)I_2 - \frac{N}{R}(V_1+V_2) \\ I_{in} = I_1 + I_2 \\ V_o = V_1 + V_2 \end{gathered} \quad (7)$$

This can be achieved by producing input currents for each converter in such a way that while the current through one inductor is rising, then its dual (i.e. the current through the other inductor) is falling at the same rate (see e.g. [13]). It can be easily verified that the slope of the current ripple of each converter can be computed as

$$\Delta I_1 = \frac{V_{in}}{L_1}D_1T \quad (8)$$

and

$$\Delta I_2 = \frac{V_{in}}{L_2}D_2T \quad (9)$$

Then for desired voltage gain we can select nominal duty cycles as complementary, and consequently,

$$D_2 = (1-D_1) \quad (10)$$

then we can achieve a *minimum ripple point* by imposing

$$\Delta I_1 = \Delta I_2 \quad (11)$$

and selecting L_1 and L_2 in such a way that they satisfy such constraint, which can be equivalently expressed as

$$L_2 = L_1\frac{(1-D_1)}{D_1} \quad (12)$$

III. Control Design

In this section, we use the model that has been derived in the previous section for a closed-loop implementation. We aim at compensating disturbances around the nominal minimum ripple point that has been used to design the converter. This implementation has potential applications in battery-fed systems, PV panels, constant power loads, and so forth. In order to design a controller, it is enough to derive a *small-signal model* that is able to predict the dynamics around the nominal minimum ripple point. This model can be obtained by the approximate linearization of the converter around the operating point, adopting the form

$$\frac{d}{dt}\hat{x} = A\hat{x} + B\hat{u} \quad (13)$$

and the to-be controlled output as

$$\hat{y} = \hat{V}_1 + \hat{V}_2\,, \quad (14)$$

where $\hat{}$ characterizes (small-signal) incremental values.

In order to compensate steady-state disturbances, we can add an integrator of the form

$$\frac{d}{dt}\omega = \hat{y} \quad (15)$$

In this way, we will have a matrix for each converter in terms of the state variables as shown in equation (13)

$$\frac{d}{dt}\begin{bmatrix}\omega\\ \hat{\imath}\\ \hat{v}\end{bmatrix} = \begin{bmatrix}0 & 0 & 1\\ 0 & 0 & \frac{-(1-D)}{NL_1}\\ 0 & \frac{(1-D)}{C_{eq}} & \frac{-N}{RC_{eq}}\end{bmatrix}\begin{bmatrix}\omega\\ \hat{\imath}\\ \hat{v}\end{bmatrix} - \begin{bmatrix}1\\0\\0\end{bmatrix}v_{ref} \quad (16)$$

From (7) in steady-state we can obtain the nominal minimum ripple point for each converter and those values are the references for the control loop.

Then we can define a state space feedback for each converter, e.g.

$$\hat{D}_1 = -k_1\omega - k_2\hat{I}_1 - k_3\hat{V}_1 \quad (17)$$

And analogously for $\hat{D}_2$. The gains can be easily computed by applying any linear control technique. According to these, the final control implementation is shown in Fig. 2.

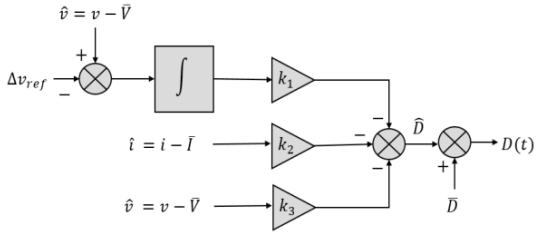

Fig. 2. Final control implementation

IV. Simulation Results

In this section, we present the validation of the topology through simulations, presenting the total gain of the converter, the ripple cancelation, and the control theory. As we can see in Fig. 3, the output voltage is almost ten times the input voltage (V_{in} =24 V), which is a high gain for a converter. According to the equation (12) the value of the duty cycle is calculated from the inductors values, which are obtained considering a continuous mode of operation, in that way the point for a total cancellation in the input current ripple is when D_1 = .287, nevertheless at this point of operation the output voltage differs from the reference, so the control moves the operation point, as we can see in Fig. 4, at this duty cycle the input current is almost ripple free, this is presented in Fig. 5.

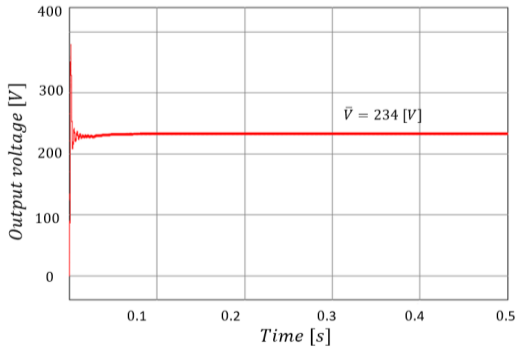

Fig. 3. Output voltage

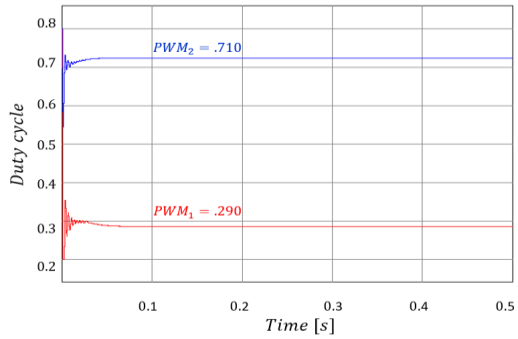

Fig. 4. Duty cycles with the control implemented

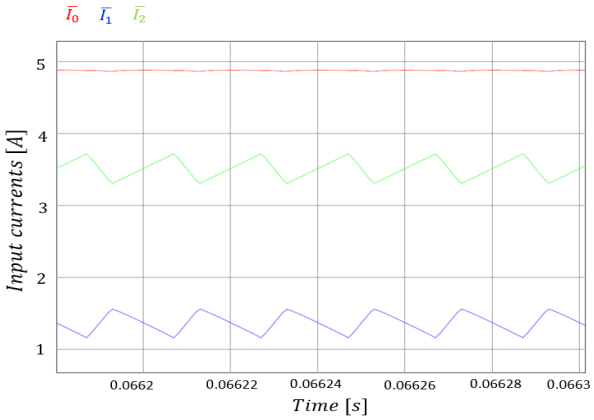

Fig. 5. Input currents with the control implemented

The controller implemented must be capable of responding over disturbances at the input voltage, as the source is expected to be a solar panel as we mentioned earlier. For this we also present a simulation where the control is validated under step disturbances, in order to see the worst case and the transient response of the system. This is presented in Fig. 6. Where we can see the time of stabilization of the output voltage and the input voltage.

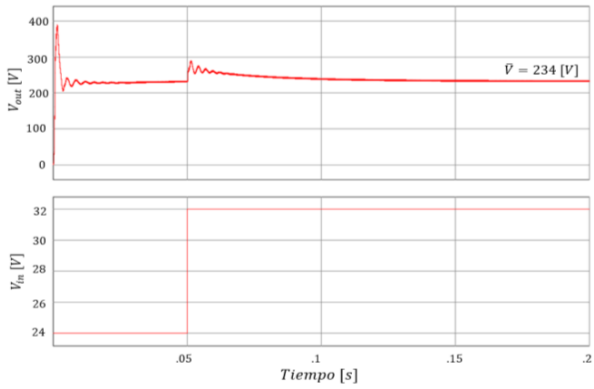

Fig. 6. Output voltage stabilization under a step disturbance

V. Experimental Validation

In order to validate the usefulness of the model and the proposed controller we implemented the topology in hardware, as shown in Fig. 7. with the list of parameters presented in Table I. We implemented the controller using a Digital Signal Controller (DSC) TI TMS320F28335. The controller gains are obtained by matrix (17) and (18), using pole placement in MATLAB, setting the poles values according to the system eigenvalues. So, the controller gains for each converter are

$$\mathbf{K_1} = [.0001, -.0101, -.0104],$$
$$\mathbf{K_2} = [.0002, -.0027, -.0016].$$

Table 1

Experimental parameters	
Parameter	***Value***
Input voltage	24 V
D_1	.287
Output voltage	232 V
F_s	50 KHz
L_1	330 µH
L_2	820 µH
C	10 µF
Mosfets	IRFP250
Diodes	BYW29E-200
Resistance	475 Ω
N	2

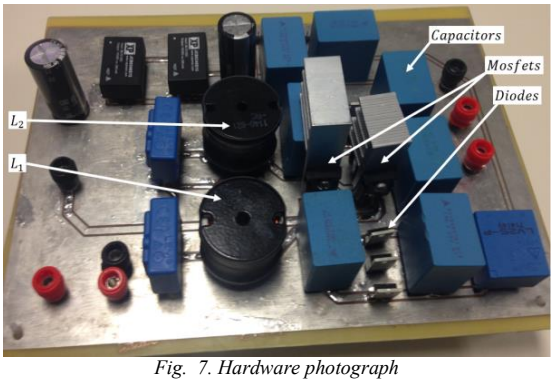

Fig. 7. Hardware photograph

Setting those gains to the control loop shown in Fig. 2, the system is controlled. In Fig. 8. we show the experimental result of the closed-loop system being under disturbances at the input-voltage, which are compensated by the controller in order to maintain a constant output voltage. As we can see, the step up was made from 24 V to 38 V, as a result the controller changed the duty cycle have a constant output voltage. At the nominal point of operation of the converter the input current should be ripple free, but as mentioned before the control moves this point in order to set the output voltage to the reference, as shown in Fig. 9. we can see an almost ripple free input current at the new point of operation, also the current from each converter is shown with their respective average values.

We can see the operation region for the converter graphically in Fig.10. where two lines showing the percentage of input current ripple are presented, one for the ripple cancelation for the traditional topologies, where the cancelation point occurs at D=.5, and the other for the topology presented here. As we can see, at the operating region, for which the converter was designed, the percentage of input current ripple, always is less than 4%, unlikely from a traditional topology where the percentage of input current ripple is more than 10%.

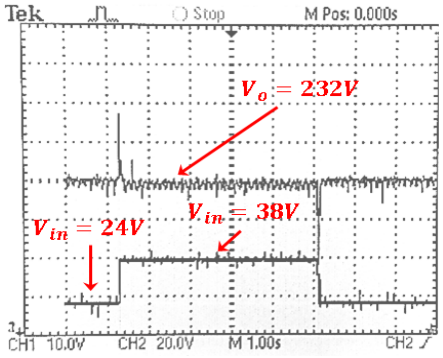

Fig. 9. Experimental results of closed-loop operation of the interleaved multilevel boost converter under step disturbances on the input voltage.

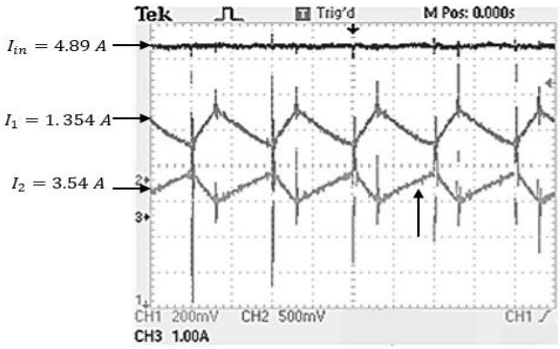

Fig. 10. Experimental results of a ripple free input current

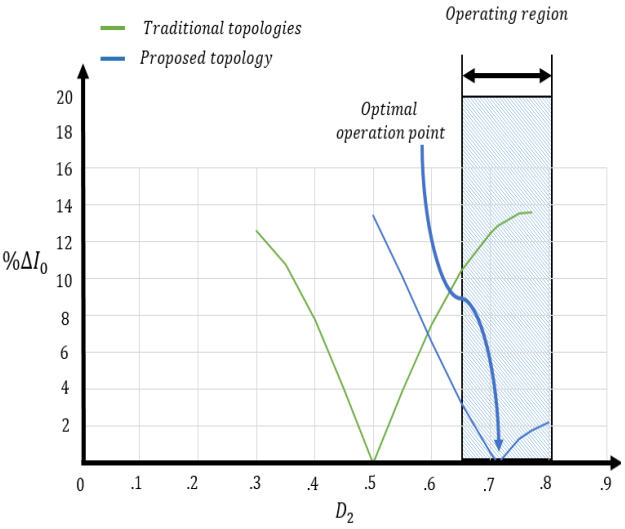

Fig. 8. Operating region for the topology presented

Another advantage of the topology presented is that the operating point is selectable, it means that according to the design parameters, the duty cycle will change, also changing the gain, in traditional topologies, where inductors sizing is equal, means moving from the optimal point where we have free ripple input current, thus limiting the gain of these topologies, nevertheless the optimal operating point of the presented topology, which depends on the inductors relation, can easily move in order to continue having the free ripple input current.

VI. Conclusion

We presented a generalized model for an interleaved multilevel boost converter that exhibits high input-to-output voltage gain and current ripple cancellation at a selectable duty cycle, these features make it ideal for renewable energy sources. The interleaved features plus the relation within inductors allows selecting the duty cycle, so the input current ripple is almost zero. The proposed model exhibits low complexity which makes it suitable for control design. The model was validated via experimental results of a closed-loop operation, where we obtain an input current with no ripple, and a constant output voltage under step disturbances.

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Chapter 9

Conclusions

Along this dissertation the modeling and control of emerging DC-DC power converters, considering their application to renewable energy sources were presented. This dissertation was not limited to a single topic, making it a compilation of applications in the power electronics field to renewable energy.

The hybrid inverter DC-DC conversion stage was improved by considering emerging topologies instead of conventional topologies. Nevertheless, the use of these emerging topologies brought challenges associated with their modeling. Added to this, the own nature of renewable energy demands the incorporation of a proper output voltage controller. The output voltage controllers presented in this work, proved that even when the system is subjected to disturbances, the output voltage value remains constant. The controllers employed were designed in continuous and discrete time. In the latest, for the discrete-time controller, a new tuning methodology technique was discussed, ensuring the stability of the system. Finally, the proposed techniques were proved in a fuel cell. The results obtained from this fuel cell represent an improvement to renewable energy exploitation.

An emphasis was made in the current ripple cancellation, since it is a pretty common problem when dealing with these sources. Different controllers were applied to the DC-DC converters proposed, the experience gained in this process is invaluable, since it allow to have a good understanding of the control design. The laboratory work done to have these experiments allow the author to have a complete understanding on the design considerations to take into account in the power electronics field.

The computational resources used in this dissertation allow the author to have a complete experience, starting from the design point and finishing in the experimental set-up. All the experimental results proved consistency with the theoretical findings presented.

9.1 Contributions

The main contributions of this work can be summarized as follows:

- A new approach was adopted to guarantee current-ripple cancellation for which duty

cycles are not constrained as in the strategies currently available in the literature, in this technique it is proved that the active minimum input-current-ripple point tracking (MRCPT) implementation permits a minimum current-ripple despite of a variable operating point.

- A new stability condition and a gain tuning methodology for the controller were design in such way to guarantee stabilization and constant output voltage.
- The proposed ripple cancellation technique was proved in a fuel cell emulator, demonstrating that the technique is applicable to renewable energy, with the advantages of improving the lifetime and efficiency of the system.
- The proposed energy administration for electric vehicles improved the utilization of ultracapacitors. Helped in both, to reduce the waste of energy, and in the acceleration process.
- DC-DC converters under instability conditions, like feeding a constant power load, was also studied. It was proved that is possible to have a stable system by means of a controller action.
- The modeling of DC-DC converters that are suitable to renewable energy is studied in such way that, even if the number of components increases, the model of the converter is similar to the very basic form of the topology. Reducing the complexity of the model.

9.2 Future work

Some future work for the topics of this dissertation are presented below:

- The proposed techniques shown in this dissertation were applied to a step-up stage, however, the same techniques are applicable to another type of converters, i.e. step-down converters or power converters that change polarity.
- The efficiency of the converters, and the overall system while using MCRPT technique was not recorded. Since efficiency is one of the main motivations when a real implementation is develop, this parameter must be registered when using this technique.
- The Minimum Current-Ripple Point Tracking (MCRPT) technique may find more applications. The condition that this technique implies, is applicable to the output voltage of converters, by designing the output capacitors in a similar way a ripple-free output voltage can be obtained.
- The MCRPT technique has been never tested using a real solar panel, and it will be interesting to test it in combination with the well-known Maximum Power Point Tracking technique.
- The MCRPT technique was applied to a interleaved converter form by two converters. It may be interesting to explore the possibility of doing a similar controller for interleaved converters with more stages.

- Since it is possible to combine the MCRPT technique with other control strategies, it is still an open topic to prove this technique with other type of controller.
- In the renewable energy technology field, the Modular Multilevel Converters MMC have gain attention in recent years. In this topic, these converters present advantages like the modularity, a low THD, the lack of a boost capacitor at the input, between others. Recently this MMC topology has been combined with storage system devices, in consequence a DC-DC converter is incorporated on each submodule of the MMC, in such case the MCRPT technique may be applicable to improve the efficiency of the overall system.
- The author is motivated in the MMC study field and is looking forward to work in this matter in the future.

Curriculum Vitae

Carlos Alberto Villarreal Hernández was born in Salamanca, Guanajuato, México, on January 30th, 1992. He received the B.S. and M.Eng. degrees in electrical engineering from Tecnológico de Monterrey, Mexico, in 2015 and 2017 respectively. He was accepted in the Ph.D. program Sciences and Engineering in August 2017. He received his Ph.D. degree from Tecnológico de Monterrey, Mexico in 2021. His research interests include power electronics and energy conversion with application on renewable energy sources. He is currently working in power electronics at the Intel laboratory in Zapopan, Jalisco.

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