INSTITUTO TECNOLOGICO Y DE ESTUDIOS SUPERIORES DE MONTERREY

MONTERREY CAMPUS

GRADUATE PROGRAM IN MECHATRONICS AND INFORMATION TECHNOLOGIES

TECNOLÓGICO DE MONTERREY®

DESIGN AND IMPLEMENTATION OF A CMOS INTERFACE FOR NON-INVASIVE OPTICAL BIOSENSORS

THESIS

PRESENTED AS A PARTIAL FULFILLMENT OF THE REQUIREMENTS FOR THE DEGREE OF

MASTER OF SCIENCE WITH MAJOR IN ELECTRONIC ENGINEERING (ELECTRONIC SYSTEMS)

BY

EDUARDO ANDRES BARREDO OCHOA

MONTERREY, N.L., MEXICO. DIC, 2009

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To my parents who are always supporting me. To my sisters who have been giving all I need all these years. To all my friends who are in Ecuador making my holidays worth. To all does people that I have met in the last six year in Mexico making my instance great.

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Eduardo Andres Barredo Ochoa

Instituto Tecnológico y de Estudios Superiores de Monterrey
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Eduardo Andrés Barredo Ochoa, M.S.
Instituto Tecnológico y de Estudios Superiores de Monterrey, 2009

Thesis Advisor: Sergio Omar Martínez Chapa, Ph.D.

Abstract

In this thesis, I propose an optoelectronic interface as those required in non-invasive micro sensors. The interface was implemented on a 0.35µm CMOS technology and consists of a photodiode to capture and transform light into a current, and an amplifier to convert this current into a voltage level.

I have designed three different photodiodes. Because of their structures, they are called p+/nwell, n+/p-substrate, nwell/p-substrate photodiodes. Additionally, I have implemented the spatially modulated technique in order to increase the photodiodes bandwidth. The required ring to avoid interference and to protect the input pads had also been incorporated in the layout.

I have reviewed mathematical approximations that describe the photocurrent in the frequency domain. These approximations could be used in later studies aimed to characterize photodiode.

Finally, the amplifier consists on a current to voltage conversion, a bandwidth expansion module and a voltage amplifier. The amplifier has showed a transimpedance of $47\,{}^{V}/_{mA}$, a frequency bandwidth of 852MHz and a gain-bandwidth of 2GHz.

Contents

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Chapter 1

Introduction

A non-invasive sensor is the one which does not produce any perturbation in the measured system. In the case of biological systems, this perturbation is related to pain or infection.

Light provides a useful technique to get information about physiological parameters. Biosensors using light are considered non-invasive.

The optical interface of this kind of sensor consists of two blocks, a photodiode and an amplifier. An electric diagram of an optical sensor is shown in the Figure 1.1. In this figure, the triangular block represents the amplifier, and the resistance R_f the amplifier factor.

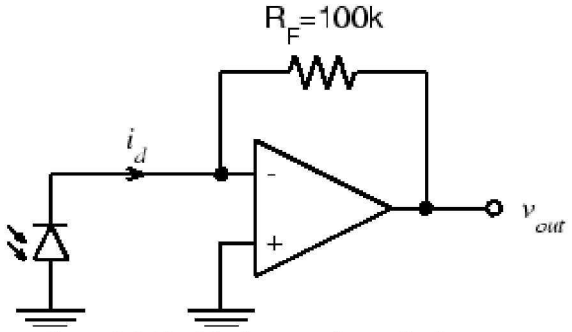


Figure 1.1: Electric diagram of an optical sensor.

It is a challenge to make a long lasting non-invasive biosensor. Researchers believe that miniaturizing the biosensor can reduce costs and obtain higher device longevity.

One step to miniaturize the optical biosensor is miniaturizing the phototransistor or photodiode. It can be done by using Complementary Metal and Oxide Semiconductors (CMOS) technology (1). It would be very useful because transistors can be made with the same process. This means that the same integrated circuit contains the photodiode and the amplifier.

Near-Infrared Spectroscopy (NIRS) are used to analyze the signal frequency behavior when the incident light is close to the near infrared range. That means when the wavelength range is 800nm-2.5µm.

1.1. Problem Statement

The BioMEMS Research Group at Instituto Tecnologico y de Estudios Superiores Monterrey (ITESM), Monterrey Campus is developing an insulin supply system.

Therefore, it will be very useful an optical biosensor to watch and control the glucose levels in diabetes patients.

Control the glucose level and automate the supply of insulin would be very helpful for the patients who suffer diabetes because this way they can optimize the use of insulin and they could supply insulin whenever is needed. To close the closed-loop control system it is necessary a biosensor which sense the glucose level. The control system can be represented as shown in Figure 1.2.

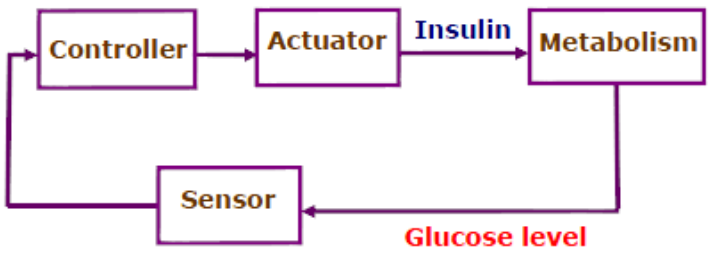


Figure 1.2: Control system of the glucose level.

The biosensor has to be sensible to the concentration of molecules of glucose to give an electronic signal which represent this concentration.

1.2. Objectives

The main objective of this thesis is to design a miniaturized optical sensor with CMOS technologies, and the electronic circuit needed to sense an optical signal. The sensor will be needed by the BioMEMS Research Group to develop the glucose control in diabetes patients. The specific objectives of this thesis are:

- Research the photodiode behavior in order to find a way to simulate its operation.
- Understand its limitations due to a technology and process constraint.
- Research photodiode layout techniques.
- Design different photodiodes layouts.
- Incorporate the layouts of the pads in order to fabricate photodiodes.
- Research the main characteristics of the amplifier that will to sense the photocurrent.
- Look for different topologies of the amplifier to obtain high bandwidth.
- Capture and simulate the amplifier.

1.3. Thesis outline

This thesis is organized in five chapters. The distribution of these chapters is as follow.

Chapter 1 presents an overview of the problem, introduction of the most important concepts; and the main and specifics objectives.

Chapter 2 describes the state of the art of optoelectronic interfaces. This chapter shows the previous work related with the optical electronic interfaces.

Chapter 3 describes the way to implement photodiodes with a CMOS technology. This chapter also reviews mathematical approximations that describe the photocurrent in the frequency domain.

Chapter 4 shows the design of the optoelectronic interface captured and simulated. The first part shows three different kinds of photodiodes with all the layers needed. The second part shows the design of the amplifier with the equations, considerations and specifications. The chapter also includes simulations of the amplifier stage.

Chapter 5 has the conclusions and future works related with this thesis.

Chapter 2
State of the art

This chapter presents some previous investigations related with this thesis. The applications optoelectronic interfaces in a sensor are many, but they can be divided in two approaches: Those interfaces that are related to spectrometry and those related to image capture.

Concerning the first approach, the objective is to get the spectrum of a signal in the frequency domain. Concerning the second approach, the goal is to obtain different readings or scans of luminance and chrominance in space domain.

Yu-Wei Chang et al (2) have designed a high-sensitivity CMOS-Compatible system. They designed a complete optoelectronic interface to sense physiological parameters like H_2O_2, histamine and glucose. A diagram of the CMOS optical biosensing system is shown in the Figure 2.1.

Chang et al (2) has designed a p+/nwell photodiode with two rings used to keep it out of noise. The Figure 2.2 and Figure 2.3 show the photodiode layout and the amplifier schematic. A better explanation of the p+/nwell photodiode design is shown in the next chapter 4.

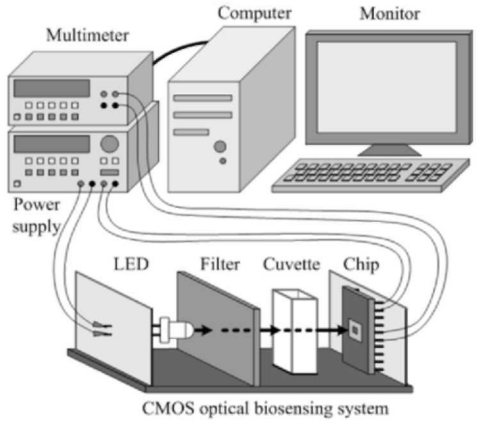


Figure 2.1: Diagram of the miniature CMOS optical biosensing system (2).

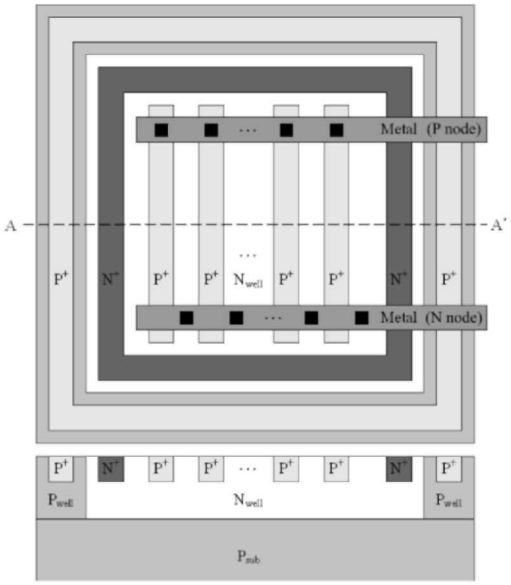


Figure 2.2: P+/nwell Yu-Wei's photodiode(2).

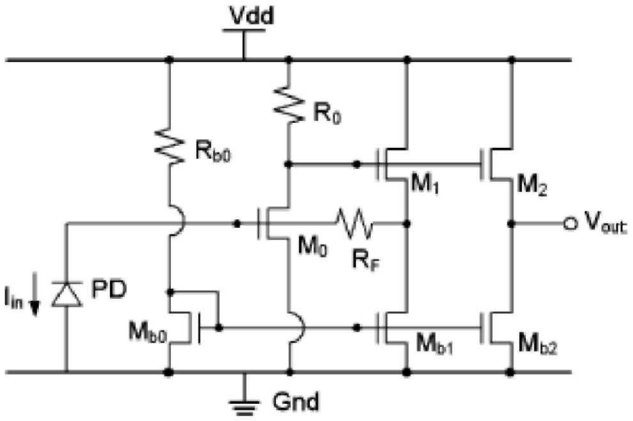


Figure 2.3: Yu-Wei's circuit amplifier (2).

Jan Genoe et al (3) designed a spatially modulated light detector (SML-detector). It consists in a nwell/p-substrate photodiode with a extra layer of metal over the half of nwell's fingers. Figure 2.4 shows the SML-detector.

The graphic on the right of the Figure 2.4 shows the normalized responsivity as a function of the bit-rate. A flat I-D curve is obtained up to 500 Mb/s.

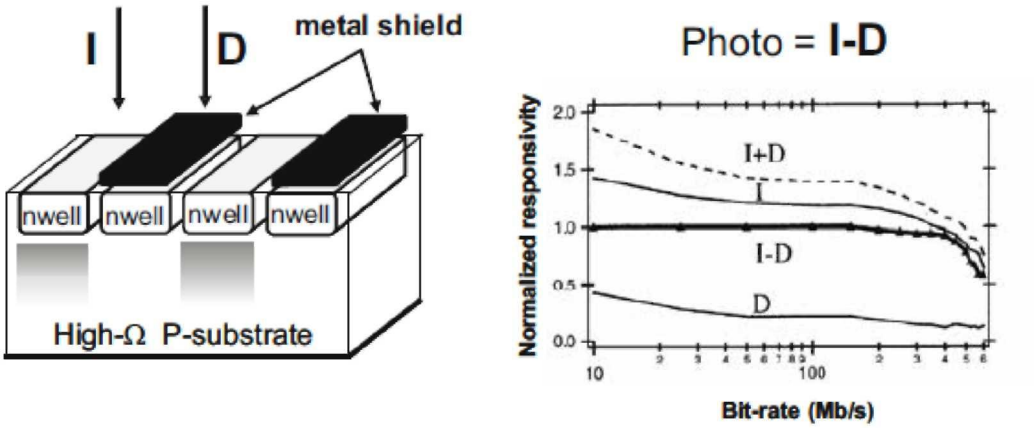


Figure 2.4: Spatially modulated light detector

Figure 2.5 shows the bandwidth of the SML-detector. The bandwidth is much higher than the conventional CMOS photodiode.

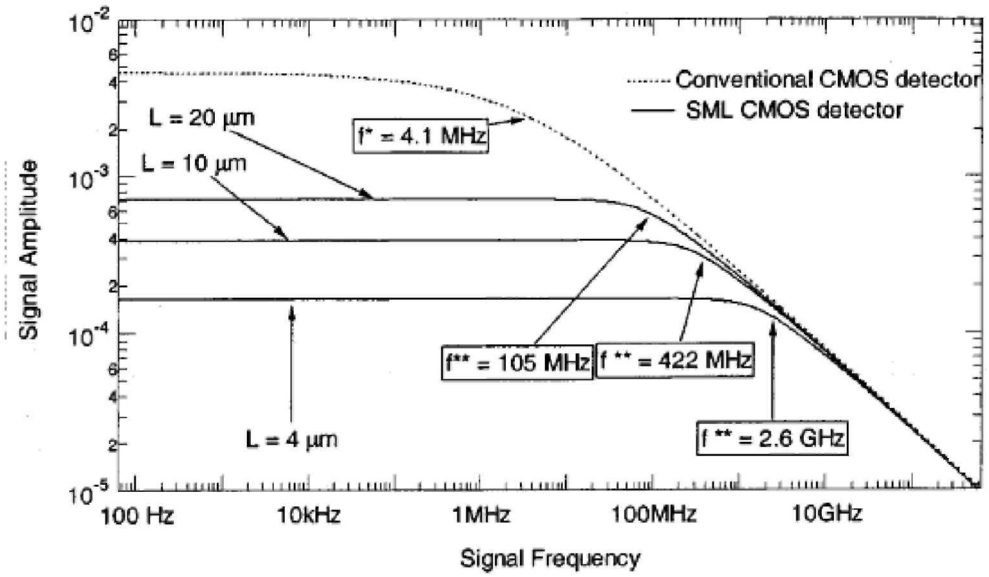


Figure 2.5: Bode diagram of the SML-detector electron current response compared to the conventional CMOS detector (dashed line).

Cheng Xu et al (4), shows the design of an Active Pixel Sensor (APS) using a CMOS technology of 0.25µm. In order to capture an image, a matrix of APS is needed. The Figure 2.6 shows the schematic circuit of one pixel.

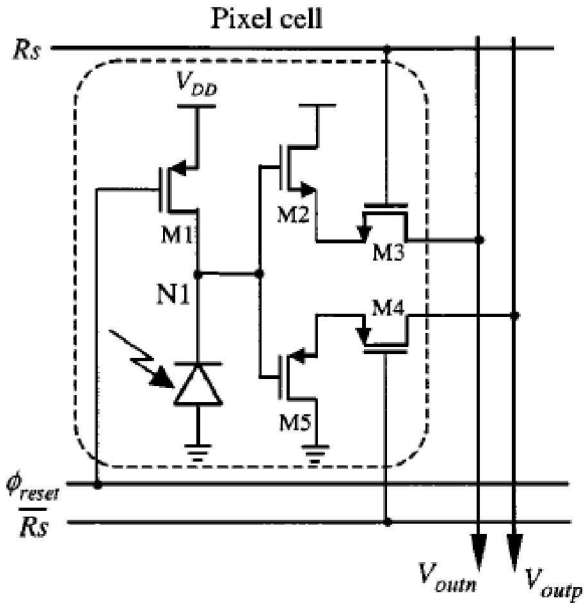


Figure 2.6: Structure of Complementary APS architecture (4).

A layout of the APS designed by Cheng Xu et al is appears in Figure 2.7. The fill factor (the relation between the entire APS and the photodiode) is 30%.

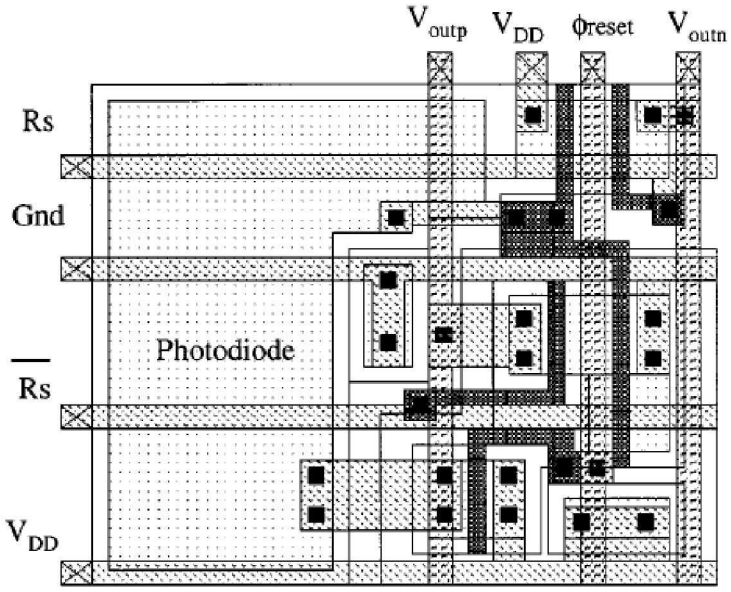


Figure 2.7: Layout of a complementary APS with a 0.25µm CMOS technology.

Alexander Fish et al (5), designed a selft-powered CMOS Active pixel sensor (SPS) architecture. The idea is to use a photodiode for self power generation. The element to provide the power to the system is called power generation photodiode (PGPd). A schematic diagram of a SPS general architecture is shown in Figure 2.8.

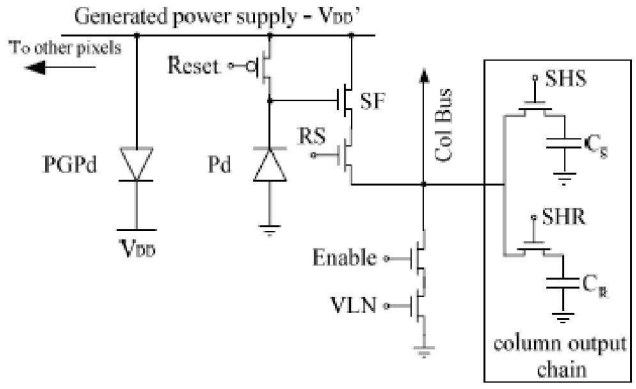


Figure 2.8: SPS general structure (5).

An implementation of a possible SPS is shown in Figure 2.9. In this photodiode application a backup circuit is necessary because the power photodiode depends on illumination levels. A. Fish (5) designed a backup circuit which appears in Figure 2.10.

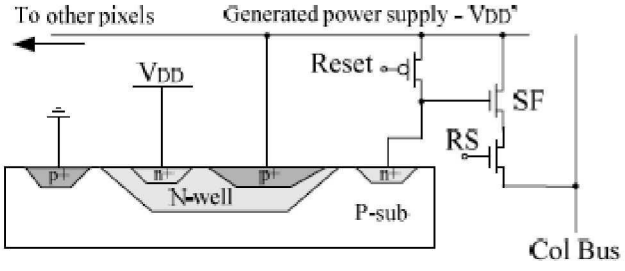


Figure 2.9: Possible SPS implementation (5).

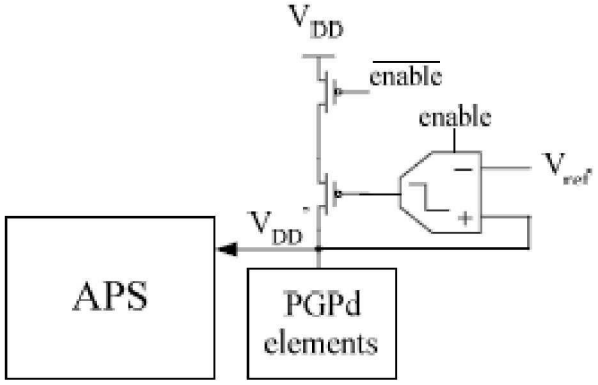


Figure 2.10: Photodiode backup circuit (5).

Markus Grözing et al (6) designed a front-end amplifier for integrated differential photodiodes. The technology used by them was a 0.18µm CMOS technology. The differential photodiode consist of a pair n+/nwell/p-substrate photodiodes connected together having a metal shading mask over one of the two photodiodes. The Figure 2.11 shows a diagram with the pair of photodiodes.

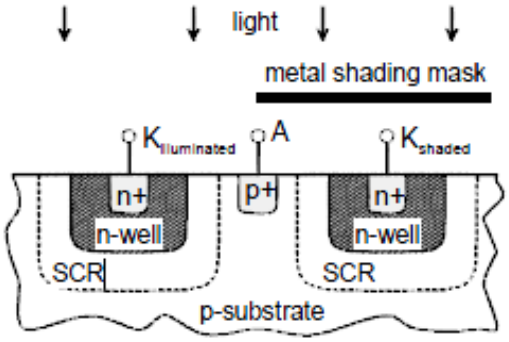


Figure 2.11: Differential photodiode pair (6).

A schematic of the differential amplifier appears in Figure 2.12. The circuit consists of a low-noise transimpendace amplifier (TIA) connected to a high-gain limiting amplifier (LIA). The output driver reduces the output impedance. The TIA converts the current to voltage, the LIA amplifies the voltage signal and the driver provides low output impedance.

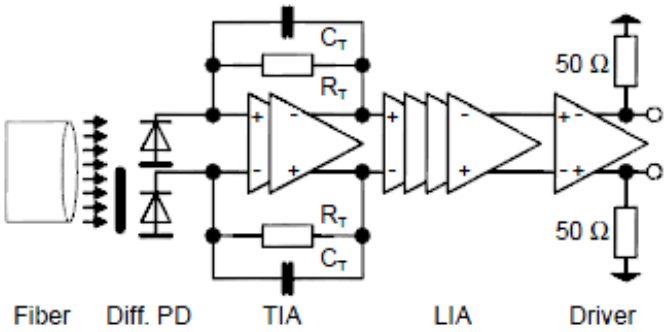


Figure 2.12: Amplifier for a differential photodiode (6).

As was explained before, spectroscopy is very useful to obtain information about different parameters. But unfortunately the silicon does not have a good performance for wavelength higher than 0.95µm. This limitation has found new interest in researchers to find other semiconductors such as GaAs (Gallium Arsenide) to provide better performances at higher wavelengths.

Tatsushi Nakahara et al (7) proposed an hybrid photodiode which consists of using both, a silicon CMOS, and a GaAs wafers. To integrate both wafers, a polyimide layer is used as shown in Figure 2.13.

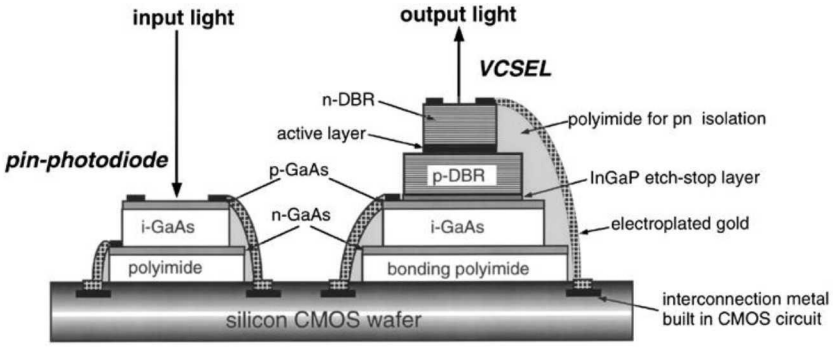


Figure 2.13: Proposed hybrid structure of CMOS/PD/VCSEL (7).

CMOS technologies are very popular for designing optoelectronic interfaces mainly because the cost of the integrated circuit. Moreover, CMOS technologies allow a monolithic solution incorporating photodiodes and circuits in the same chip.

CMOS sensors became very popular for image capture. Nowadays, they are incorporated in video cams. Concerning spectrometry, the silicon is limited to wavelengths in the range from 400nm to 1µm. Anyway, it is possible to design high bandwidth optoelectronic devices using silicon.

It is also important to mention that photodiodes could be used to design autonomous devices by generating some electrical micro power from light. This will allow further device miniaturization by eliminating batteries.

Finally, researchers are investigating hybrid Si/GaAs optoelectronic interfaces. The importance of this approach is to have the best of two different technologies, from CMOS the cost and compatibility and from GaAs the wavelength response of the photodiode.

Chapter 3

Photodiode with a CMOS technology

This chapter shows different photodiodes that can be made using a Standard CMOS technology. There are several alternatives of photodiode designs and each one has advantages and disadvantages.

The chapter is divided in two main parts: First, the diode is analyzed as an ideal device. This allows the characterization of the most important device parameters having the light source as an input and the photodetector as the sensor/processor of information. In the second part, CMOS photodiodes are presented. Some parameters are discussed in detail such as the bandwidth, photodiode capacitance, input impedance and frequency response.

Most of the contents of this chapter has been synthesized from the book "*High-Speed Phodiodes in Standard CMOS Technology*"(8).

3.1. Introduction

The light is only a part of the electromagnetic (EM) spectrum. The difference in radiation can be measured using quantities such as wavelength, frequency of the EM wave and energy of photons. Depending on which part of the spectrum is analyzed, a different light quantity is considered in more detail.

In optics, the most commonly used light quantity is wavelength, measured in micrometers or nanometers. The Figure 3.1 shows the EM spectrum with the wavelength in each range.

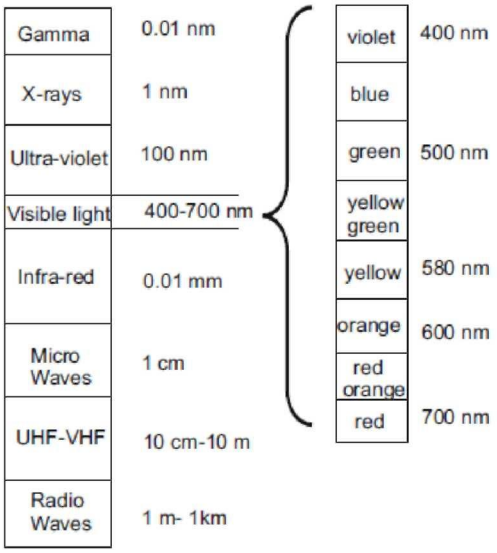


Figure 3.1: Electromagnetic spectrum.

A light beam can be seen as a sinusoidal wave than travel in space with certain speed. In fact, this speed is the light speed and it is equal to $c = 299{,}792{,}458\text{m/s} \approx 3\text{x}10^8\text{m/s}$.

The wavelength is the displacement of the wave in a period, and it is inversely proportional to the frequency of this wave:

$$\lambda = \frac{c}{f} \tag{3.1}$$

3.2. Ideal photodiode

In general, a photodiodes is a solid state transducer used for converting light energy into electrical energy. The main requirements of the ideal photodiodes are:

- To detect all incident photons.
- Bandwidth is larger than the one of an input signal.
- To have noise immunity.

The photodiodes work in the diode reverse biased zone. They work with a fix inverse bias voltage (VB) on their terminals and the photocurrent will be modulated by the incident light. The Figure 3.2 shows the photocurrent as a function of voltage for three different levels.

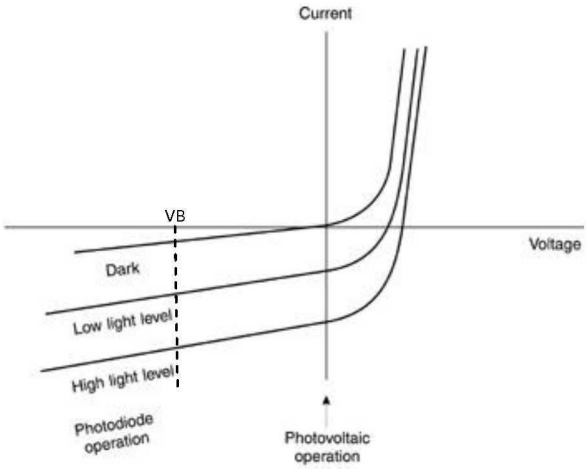


Figure 3.2: Characteristic curve of the photodiode.

Note that the photodiode delivers a current even when no light is available. That current is called "dark current".

3.3. Absorption light in silicon

In the process of light absorption, part of the photons is absorbed into the material. The light-intensity (I) decrease exponentially with distance into the material: (9)

$$I \; \alpha \; e^{-\beta x} \tag{3.2}$$

Where β is the absorption coefficient that depends upon of the wavelength (λ) of silicon (10).

$$\beta = 10^{13.2131 - 36.7985\lambda + 48.1893\lambda^2 - 22.5562\lambda^3} \tag{3.3}$$

and λ is given in micrometers [μm].

Photodiodes designed with a CMOS technology are sensitive only for a particular wavelength range. In silicon at large wavelengths, $\lambda > 950\ nm$, the photon energy is not high enough to create an electron-hole pair. On the other hand, for low wavelength, $\lambda < 400\ nm$, excess carries are generated very close to the photodiode surface.

Another parameter of interest is the depth when the intensity of the light decay to $1/e$ of the incident-light. This depth is named $1/e$ absorption depth and is equal to $1/\beta$.

Figure 3.3 shows the absorption coefficient α and $1/e$ absorption depth as a function of the wavelength of the incident light.

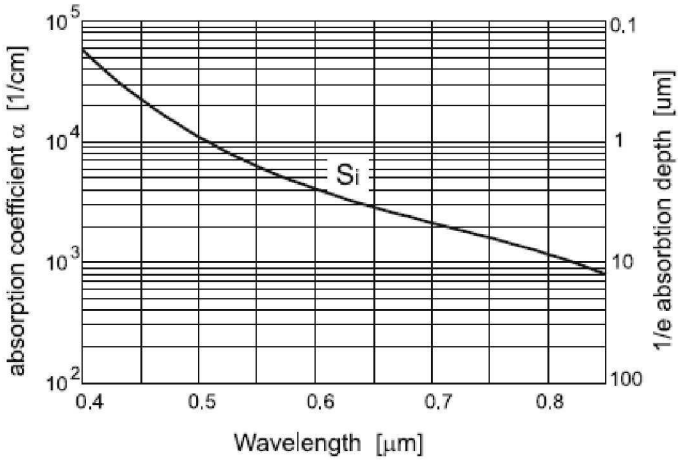


Figure 3.3: Absorption coefficient β versus wavelength.

Once the light reaches the surface, it decreases exponentially:

$$\frac{\partial I}{\partial x}\alpha\ \beta e^{-\beta x} \tag{3.4}$$

Now we can define $G(x)$ as the carrier generation rate with the following equation.

$$G(x) = \Phi_0 \beta e^{-\beta x} \tag{3.5}$$

Where Φ_0 is the photon flux and it can be expressed as:

$$\Phi_0 = \frac{P_{in}}{h\upsilon}(1-\Gamma) \tag{3.6}$$

P_{in} is the incident power at the surface, h is the Plank constant, υ is the frequency of the photon and Γ is the reflection coefficient (9).

3.3.1. An easy approach of the photocurrent

In order to determinate the current generated by the incident light, we can define the term $\frac{P_{in}}{h\upsilon}$ as the numbers of photons arrived for a given υ frequency. The number of generated carrie pairs is closed to $\eta\frac{P_{in}}{h\upsilon}$ where η is the *quantum efficiency*. Finally the photocurrent is closed to$\eta e\frac{P_{in}}{h\upsilon}$ where e is the electron charge (9).

Now we define the photodiode *responsivity*, it is the average photocurrent per unit of incident power:

$$R = \frac{e\eta}{h\upsilon} \tag{3.7}$$

To find an equation of responsivity in terms of the wavelength use equation 3.1 and make$f = \upsilon$, therefore:

$$R = \frac{e}{hc}\lambda\eta(\lambda) \tag{3.8}$$

$$R = \frac{\lambda\eta(\lambda)}{1.24} \tag{3.9}$$

Where λ is in μm. It is important not to lose the interest of this approach allow us to find an easy equation for the photocurrent. The photocurrent, therefore, can be obtained simply multiplying the responsivity by the incident power at the surface as follows:

$$i = RP_{in}A_{pd} \tag{3.10}$$

Where P_{in} is given in $^{W}/_{cm^2}$and A_{pd} is the effective photodiode area.

Analyzing the Equation 3.9, we expect higher levels of current using higher wavelengths. But the quantum efficiency also depends on the wavelength and the semiconductor type. A typical value for the quantum efficiency in a CMOS photodiode is about 40%-70% (8).

Figure 3.4 shows the responsivity as a function of the wavelength for three different semiconductors.

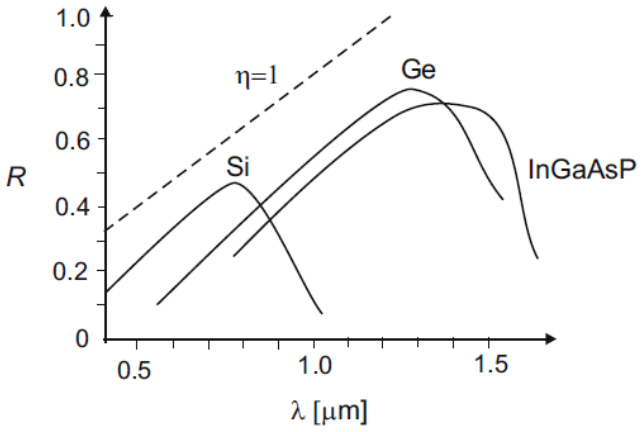


Figure 3.4: Responsivity of Si, Ge and InGaP photodiode.

3.4. Photodiode design

To understand the structures of the different CMOS photodiodes, we need to explain the CMOS technology. Figure 3.5 shows the different layers of a CMOS technology having 0.35µm as a minimum feature size using in the design of Metal and Oxide Semiconductor Field Electric Transistors (MOSFET) (11) .

The objective of this section is to describe the process of fabrications of CMOS photodiodes and transistors. In designing photodiodes, the available IC layers are the same as in CMOS transistor design.

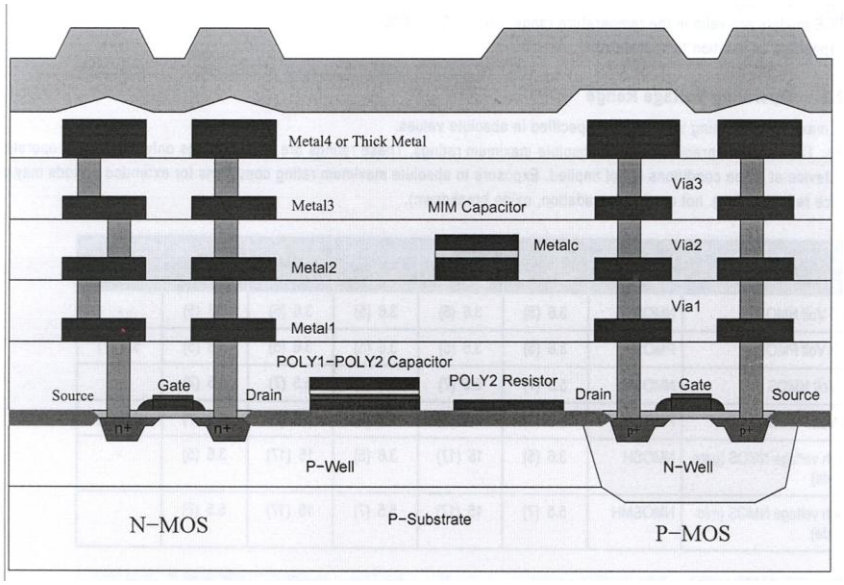


Figure 3.5: Cross view of 0.35µm CMOS technology layers.

3.4.1. Photodiodes main variants

A photodiode consists of a PN junction made from different layers of the CMOS technology. The alternative designs are:

- Nwell/p-substrate
- N+/p-substrate
- P+/nwell/p-substrate
- P+/nwell

Two different topologies are available in a standard CMOS technology with well implantation:

- Twin-well with adjoined wells
- Triple-well with separate wells

Basically, the fist scheme consists of two different wells to form two sort of transistors (PMOS and NMOS). The second scheme consist of one well, normally a nwell, and it is used to form the PMOS transistor. In the NMOS transistor the substrate functions as the well where the device is built.

Considering the substrate, two different photodiode design schemes are available (8):

- High resistance substrate
- Low resistance substrate

The low resistance substrate consists of a p+substrate under the p-epi layer, as shown in Figure 3.7 and Figure 3.10. Otherwise, the substrate is considering as "high resistance substrate". Some of these variations are shown in the Figure 3.6, Figure 3.7, Figure 3.8 and Figure 3.9.

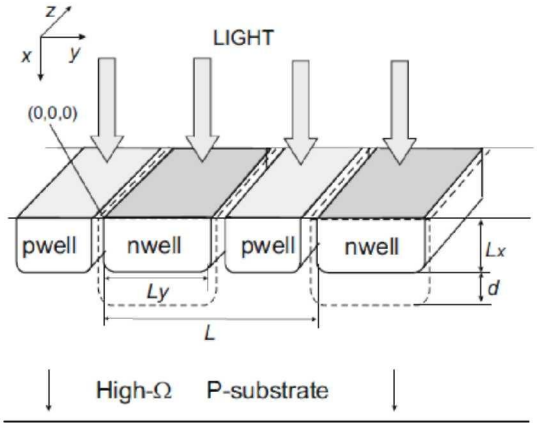


Figure 3.6: Finger nwell/p-substrate photodiode structure with high resistance substrate and twin-wells in standard CMOS technology.

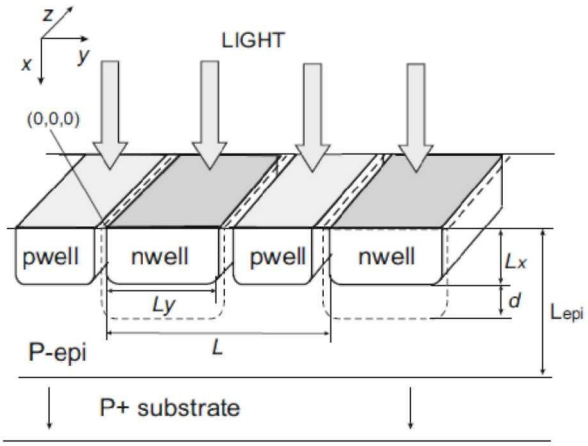


Figure 3.7: Finger nwell/p photodiode structure with low-resistance substrate and twin-wells in standard CMOS technology.

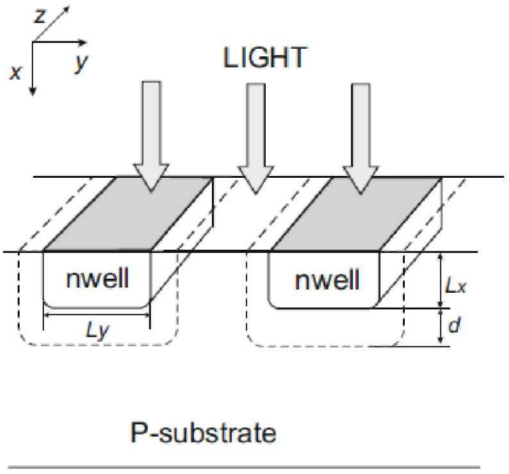


Figure 3.8: A finger nwell/p-substrate photodiode structure with high resistance substrate and separate-wells standard CMOS technology.

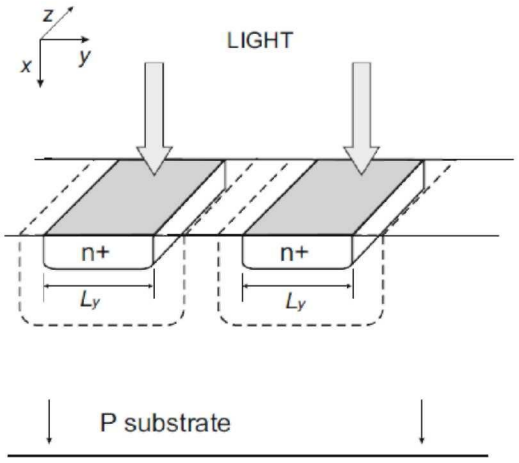


Figure 3.9: Finger n+/p-substrate photodiode with high-resistance substrate

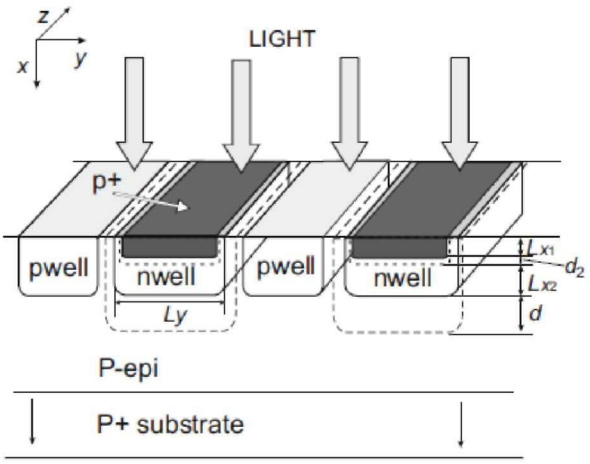


Figure 3.10: Finger p+/nwell/p-substrate photodiode structure with low-resistance substrate and adjoined-wells.

In designing the photodiodes, L_y, L are selected to maximize the bandwidth. Nevertheless, L_x, d, L_{epi} are technology dependent parameters which can not be changed.

There are two main different geometries:

- Minimal nwell/n+ width *L*ymin. Typically for standard CMOS, the minimal width is twice the nwell/n+ depth: *L*ymin=2µm.
- Nwell/n+ width much larger than the nwell/n+ depth: *Ly*=10 µm.

3.5. Bandwidth of photodiodes in CMOS

Inside the photodiode the carriers can move either by drift (inside the depletion region) or by diffusion (outside the depletion region). The photodiode current response is the sum of the drift current I_{drift} plus the diffusion currents I_{diffk} (8):

$$I_{int_{total}} = I_{diff_{nwell}} + I_{diff_{n+}} + I_{diff_{p+}} + I_{diff_{p-subs}} + I_{drift} \quad (3.11)$$

The currents of the different photodiode regions are calculated by taking the Laplace Transform of the diffusion equation in time domain (3). To obtain an estimated frequency domain behavior, the Discrete Fourier series in space domain is applied to the Laplace expression.

3.5.1. Nwell/p-substrate, high resistance and twin well technology

This section presents a frequency representation of the nwell/p-substrate photodiode structure. In this case, $I_{diff_{n+}}$ and $I_{diff_{p+}}$ are zero because n+ nor p+ material are used. A representation of this structure was presented in the Figure 3.6.

The first current to find will be the nwell diffusion current $I_{diff_{nwell}}$. This current is found using the method explained before to the diffusion equation (12):

$$\frac{\partial p_n(t,x,y)}{\partial t} = D_p \frac{\partial^2 p_n(t,x,y)}{\partial x^2} + D_p \frac{\partial^2 p_n(t,x,y)}{\partial y^2} - \frac{p_n(t,x,y)}{\tau_p} + G(t,x,y) \quad (3.12)$$

Where $p_n(t,x,y)$is the excess minority carrier concentration inside the nwell, $D_p$is the diffusion coefficient of the holes in the n-doped layer and $\tau_p$is the lifetime of the minority-carrier.

$G(t,x,y)$ can be expressed as follow:

$$G(t,x,y) = \beta \Phi_0(t) e^{-\beta x} \quad (3.13)$$

Where β is given by the equation 3.3 and $\Phi_0(t)$ by the equation 3.6.

To solve the equation 3.12, four boundary conditions for the hole-profile are required, two in each direction, x and y. The Figure 3.11 shows those boundary conditions:

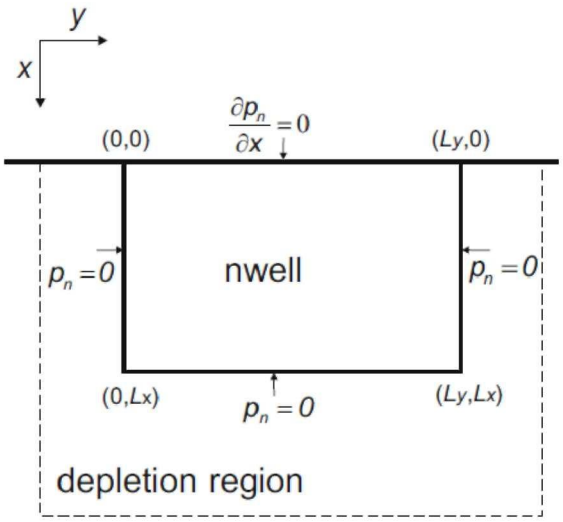


Figure 3.11: The boundary conditions for hole densities inside nwell.

Using those boundary conditions and applying Laplace Transform and Discrete Fourier series, the final expression for the nwell diffusion current is:

$$\frac{J_{nwell}(s)}{\Phi_0(s)} = 32 \frac{eL_p^2 \beta}{l\pi^2} \sum_{n=1}^{\infty} \sum_{m=1}^{\infty} (2n-1)\pi \frac{e^{-\beta L x} + (-1)^{n-1} \beta L_x}{4\beta^2 L_x^2 + (2n-1)^2 \pi^2} \frac{\frac{2L_x}{L_y}\frac{1}{2n-1} + \frac{L_y}{2L_x}\frac{2n-1}{(2m-1)^2}}{\frac{(2n-1)^2\pi^2 L_p^2}{4L_x^2} + \frac{(2m-1)^2\pi^2 L_p^2}{4L_y^2} + 1 + s\tau_p} \quad (3.14)$$

Applying some simplifications like in (3), the -3dB bandwidth frequency can be approximated with:

$$f_{3dB} \cong \sqrt[3]{\left(\frac{\lambda}{\lambda_{850}}\right)} \frac{\pi D_p}{2} \left(\left(\frac{1}{2L_x}\right)^2 + \left(\frac{1}{L_y}\right)^2 + \left(\frac{1}{L_p}\right)^2 \right) \quad (3.15)$$

L_p is the diffusion length of the holes. Typically L_p is much larger than L_y or L_x, for that reason, the contribution of third term in brackets is very small.

Equation 3.15 shows that the bandwidth can be large at higher wavelengths. But the quantum efficiency will decay if silicon is used. To develop a high speed circuit, for example in NIR range, silicon is not the best material. Perhaps Ge or InGaAsP will perform better in terms of high bandwidth and speed.

The Figure 3.12 and Figure 3.13 show the amplitude and the phase as a function of the frequency for each term of the equation 3.14.

The Figure 3.14 shows the result of the double sums for the amplitude and phase as a function of the frequency.

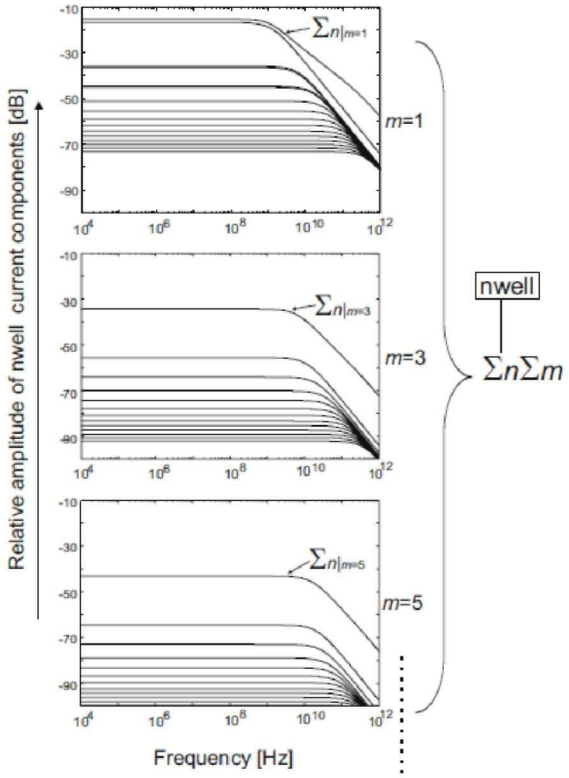


Figure 3.12: Amplitude of the double Fourier series of the nwell diffusion current for the vertical and the lateral nwell direction.

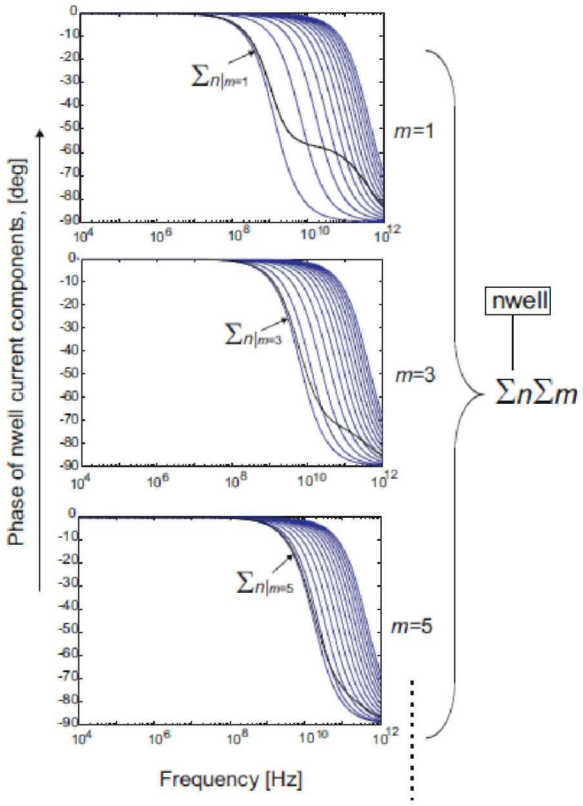


Figure 3.13: Phase of the double Fourier series of the nwell diffusion current for the vertical and the lateral nwell direction

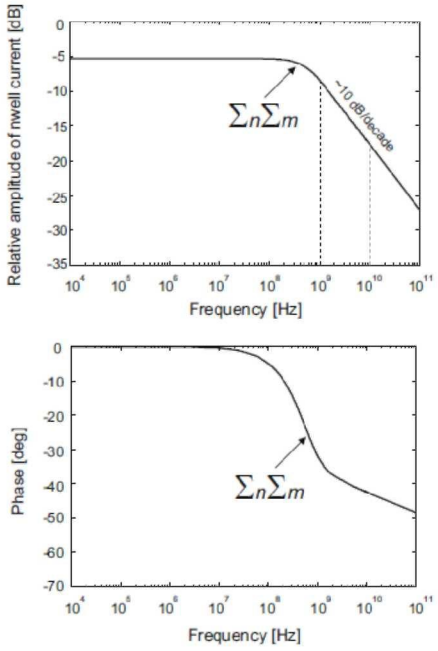


Figure 3.14: The total amplitude and phase of the nwell diffusion current.

The next step in order to find the complete bandwidth result is to find the high-resistance substrate current $I_{diff_{p-subs}}$.

The substrate current is the photocurrent resulting from generated charge below wells and between them. But the contribution of generated charge below wells is dominant. Therefore, the sidewall effects are neglected.

This current can be calculated by using a one-dimensional diffusion equation explained in (12):

$$\frac{\partial n_p(t,x)}{\partial t} = D_n \frac{\partial^2 n_p(t,x)}{\partial x^2} - \frac{n_p(t,x)}{\tau_n} + G(t,x) \tag{3.16}$$

Where $n_p(t,x)$is the excess electron concentration inside the substrate is, D_n is the diffusion coefficient of the electrons and τ_n is the minority-carrier lifetime and $G(t,x)$is given by the following equation (8):

$$G(t,x) = \beta \Phi_0(t) e^{-\beta(L_x+d+x)} \tag{3.17}$$

Once again, β and $\Phi_0(t)$ are given by the equation 3.3 and equation 3.6 and d is the depletion region length (see Figure 3.6).

The boundary conditions in this case are:

$$n_p|_{x=0} = 0 \tag{3.18}$$

$$n_p|_{x=L_{fnt}} = 0 \tag{3.19}$$

L_{fnt} is the depth where the light is almost completed absorbed (99%). In this case, for $\lambda = 850nm$, $L_{fnt} = 60\mu m$ (8).

Solving the equation 3.16 with a similar procedure like before, J_{subs} can be express as:

$$J_{subs}(s) = \sum_{n=1}^{\infty} \frac{2\beta e \Phi(s) e^{-\beta(L_x+d)} n^2\pi^2}{L_{fnt}\left(\beta^2 L_{fnt}^2 + n^2\pi^2\right)\left(\frac{s}{D_n} + \frac{1}{L_n^2} + \frac{n^2\pi^2}{L_{fnt}^2}\right)} \tag{3.20}$$

The Figure 3.15 shows the amplitude and phase of the equation above for each term of the sum and the complete sum.

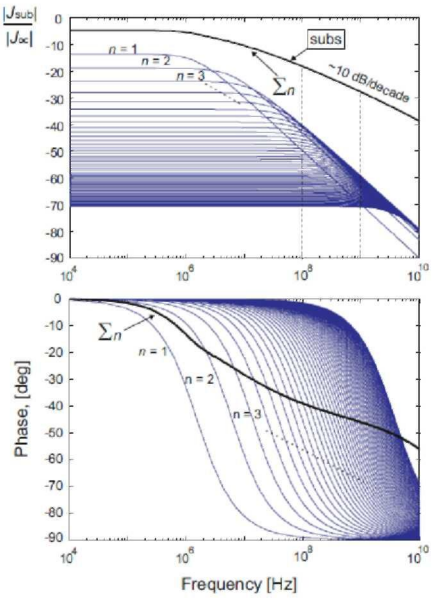


Figure 3.15: Frequency response of the substrate diffusion current

Finally, the last term of the equation 3.11 has to be found. The drift current I_{drift} is directly related to the depletion volume in which carriers are generated (8):

$$J_{drift} = J_{dep} = \Phi e\left(\left[e^{-\beta L_x} - e^{-\beta (L_x+d)}\right]\frac{A_{total}}{A_{efflat}} + \left[1 - e^{-\beta L_x}\right]\frac{A_{total}}{A_{effver}}\right) \tag{3.21}$$

Where A_{efflat} and A_{effver} are the effective lateral and vertical depletion region areas in comparison with the total photodiode area A_{total}.

The transit time of the holes and electrons inside depletion region is:

$$E_{max} = \frac{eN_A W_{tot}}{\epsilon_0 \epsilon_r} \tag{3.22}$$

$$E(x) = \xi E_{max} + \frac{x}{W_{tot}}(1-\xi)E_{max} \tag{3.23}$$

$$\upsilon_{n,p}(E) = \frac{\upsilon_{sn,sp}}{\left[1 + \left(\frac{E_{n,p0}}{E(x)}\right)^{\gamma_{n,p}}\right]^{\frac{1}{\gamma_{n,p}}}} \tag{3.24}$$

$$T_{n,p} = \int_0^{W_{tot}} \frac{1}{\upsilon_{n,p}(x)}dx \tag{3.25}$$

$$\overline{T_{n,p}} = \frac{\int_0^{W_{tot}}\left[T_{n,p}(x) - T_{n,p}(0)\right]dx}{W_{tot}} \tag{3.26}$$

Table 3.1: List of parameters.

Symbol	Meaning	Symbol	Meaning
E_{max}	Maximum electric field	ξ	Ratio between minimum and maximum electric field
e	Electron charge: $1.6\text{x}10^{-19}$C	x	Distance in the depletion region
N_A	Lighter doping concentration of the substrate	$\upsilon_{n,p}(E)$	Saturation velocity depending on E
W_{tot}	Depletion region width	$\upsilon_{sn,sp}$	Saturation velocity of holes and electrons: 10^7cm/s
ϵ_0	Permittivity of Free Space $8.8541\text{x}10^{-14}$F/cm	$E_{n,p0}$	$E_{n0} = 7000\,{}^{V}/_{cm}$ $E_{p0} = 20000\,{}^{V}/_{cm}$
ϵ_r	Relative permittivity: 11.7 for silicon	$\gamma_{n,p}$	$\gamma_n = 2, \gamma_p = 1$
$E(x)$	Electric field at x distance	$T_{n,p}$	Transit time

Using equation 3.22 to equation 3.26, the cutoff frequency can be calculated as (13):

$$f_{p,n} = \frac{2.4}{2\pi\overline{T_{n,p}}} \tag{3.27}$$

For a standard CMOS technology of 0.18µm, $f_p = 10.52GHz$ and $f_n = 46.3GHz$. Those frequencies are higher than the others two cutoff frequencies (see Figure 3.14 and Figure 3.15). For that reason the drift current will be taken as a constant in frequency domain.

The Figure 3.16 shows the three currents as a function of the frequency and the sum of them (8).

The only different between using a 10µm nwell or 2µm nwell is the nwell current curve. Notice that the maximal roll-off value is about 57 dB/decade for $L_y = 10\mu m$ and 5.2 dB/decade for $L_y = 2\mu m$

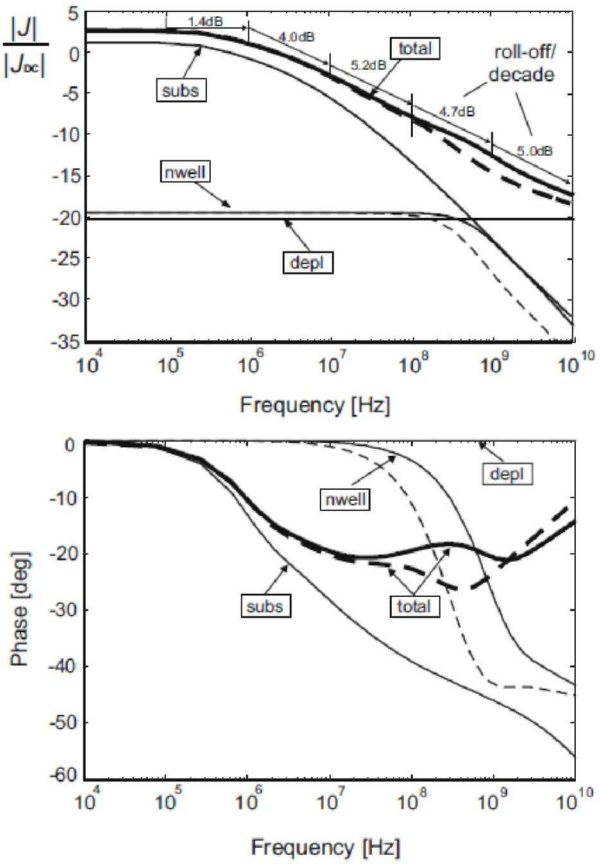


Figure 3.16: The calculated total photocurrent response of nwell/p-substrate photodiode with high-resistance substrate in a twin-well technology: 2 µm (solid lines) and 10 µm nwell size (dashed lines) for λ = 850 nm.

3.5.2. Nwell/p-substrate photodiode with low-resistance substrate and twin technology

This section will analyze a photodiode with a low-resistance substrate. To keep in mind, the designers can choose between low or high resistance substrate. The section before analyze a photodiode but with high resistance substrate. The Figure 3.7 shows a representation of this photodiode.

The only difference between this photodiode and the previous one is the substrate current response. Once again, this response can be found by using one-dimensional diffusion equation. But in this case, because there are two "p" layers, there will be two equations in order to describe the movement of the minority electrons:

$$\begin{cases} \dfrac{\partial n_{p1}}{\partial t} = D_n \dfrac{\partial^2 n_{p1}(t,x)}{\partial x^2} - \dfrac{n_{p1}(t,x)}{\tau_{p1}} + G_1(t,x) \\ \dfrac{\partial n_{p2}}{\partial t} = D_n \dfrac{\partial^2 n_{p2}(t,x)}{\partial x^2} - \dfrac{n_{p2}(t,x)}{\tau_{p2}} + G_2(t,x) \end{cases} \tag{3.28}$$

$$\begin{cases} G_1(t,x,y) = \beta \Phi_0(t) e^{-\beta(L_x+d+x)}|_{x\in[0,L_{epi}]} \\ G_2(t,x,y) = \beta \Phi_0(t) e^{-\beta(L_{epi}+x)}|_{x\in[0,\infty]} \end{cases} \tag{3.29}$$

Where L_{epi} is the depth of the p-epi layer. The procedure to find the current response is the same as the section before, but there have to be two more boundary conditions. The boundaries conditions for this problem are:

$$D_{p1} \frac{\partial n_{p1}(s,x)}{\partial x}|_{x=L_{epi}} = D_{p2} \frac{\partial n_{p2}(s,x)}{\partial x}|_{x=L_{epi}} \tag{3.30}$$

$$n_{p1}(s, L_{epi}) = n_{p2}(s, L_{epi}) \tag{3.31}$$

$$n_p|_{x=0} = 0 \tag{3.32}$$

$$n_p|_{x=\infty} = 0 \tag{3.33}$$

Using low resistance substrate instead high resistance will improve the bandwidth response, but the responsivity will decay. In others words, the photocurrent is lower but it can sense at higher frequencies. The Figure 3.17 shows the current response as a function of the frequency for a low resistance substrate (8).

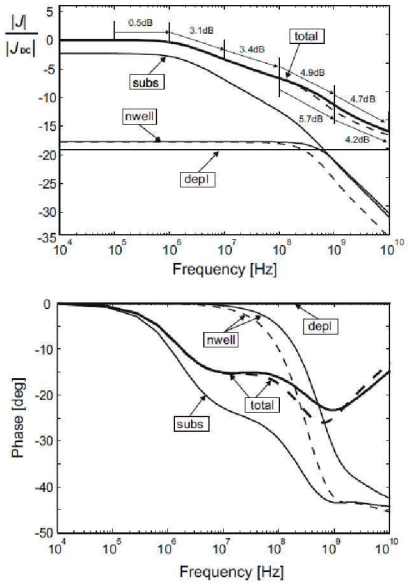


Figure 3.17: The calculated amplitude response of nwell/p-substrate photodiode with low-resistance substrate in a twin-well technology: 2 µm (solid lines) and 10 µm nwell size (dashed lines) for λ = 850 nm.

The roll-off behavior in this case is 1-2 db/decade lower than in the previous section.

Radovanovic et al, used a semiconductor parameter analyzer (SPA) HP4146B to provide the supply and bias voltage. With the SPA sensed the DC photocurrent and the frequency response of the same photodiode (Nwell/p-substrate, low-resisntance substrate, twin technology). The Figure 3.18 shows the DC behaviour and the Figure 3.19 the frequency response (8).

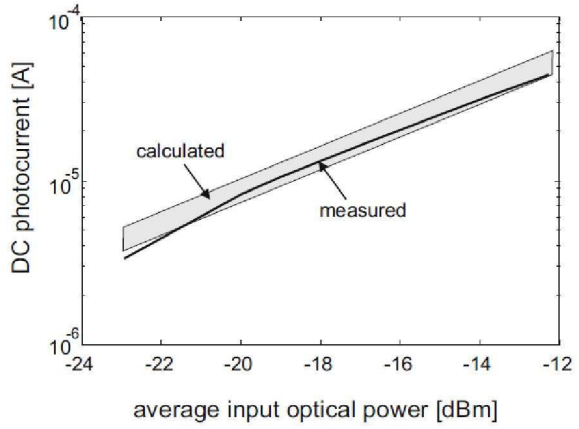


Figure 3.18: The measured DC photocurrent of nwell/p-substrate photodiode for λ = 850 nm.

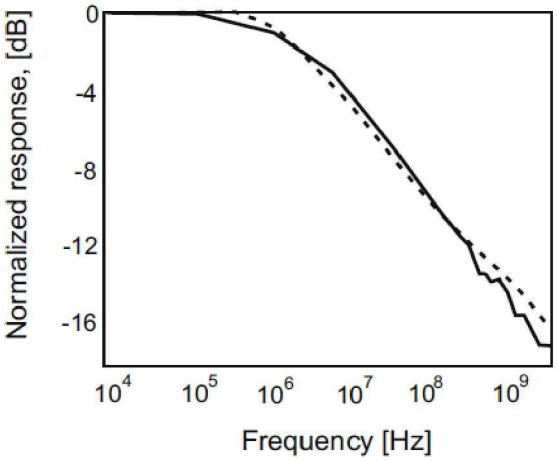


Figure 3.19: The measured (line) and calculated (dashed) responses of a nwell/p-substrate photodiode with 2 µm nwell-size, λ = 850 nm.

3.5.3. Nwell/p-substrate photodiode with high-resistance substrate and separated wells

This section and the next one have a particular interest because these kind of photodiodes can be designed at LabMEMS (laboratory of micro-electromechanical systems) at ITESM, Monterrey Campus, place where I did all my investigations and simulations. CMOS of 0.35µm technology

with separated wells and high-resistance substrate is available there, this technology was presented before by Figure 3.5.

This photodiode structure is shown in the Figure 3.8. The lateral depletion region between nwells in significantly increased. For that reason, the amplitude of the drift current response is higher. But at higher frequencies, this photodiode's roll-off is 1-2dB lower than the one with twin well technology. The Figure 3.20 shows the frequency response of this photodiode (8).

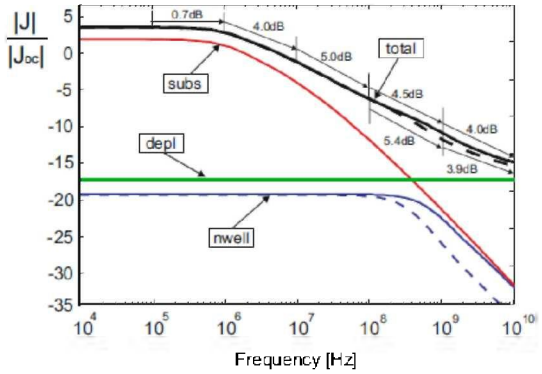


Figure 3.20: The response of nwell/p-substrate photodiode with high-resistance substrate in a separate-wells technology: 2 µm (solid lines) and 10 µm nwell size (dashed lines) for λ = 850 nm

3.5.4. N+/p-substrate with high-resistance substrate and separated wells.

This photodiode structure is shown in the Figure 3.9. The response of the n+ region is obtained by changing the values of the diffusion length L_p and diffusion coefficient D_n.

The maximum frequency response is determinate mainly by the depth of the n+ region. Since this depth is much smaller than the nwell one, the bandwidth will be smaller (8).

3.5.5. P+/Nwell/p-substrate with low-resistance substrate and adjoined wells.

This kind of photodiode is formed by two photodiodes: p+/nwell and nwell/p-substrate. The structure of this photodiode is shown in the Figure 3.10. Because of its structure, this kind of photodiodes is often referred as double photodiode.

For this problem, first the p+/nwell junction has to be solved. To find an expression to the current, the same equation for nwell/p-substrate, only changing the values of the diffusion coefficients, diffusion lengths and junction depth is used. The boundary conditions for the "second" photodiode (nwell/p-substrate) are shown in the Figure 3.21.

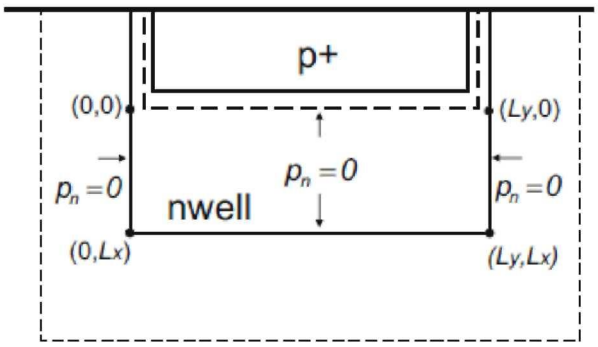


Figure 3.21: The boundary conditions for the hole density inside the nwell for the double-photodiode.

The total response at the frequency of this photodiode is shown in the Figure 3.22.

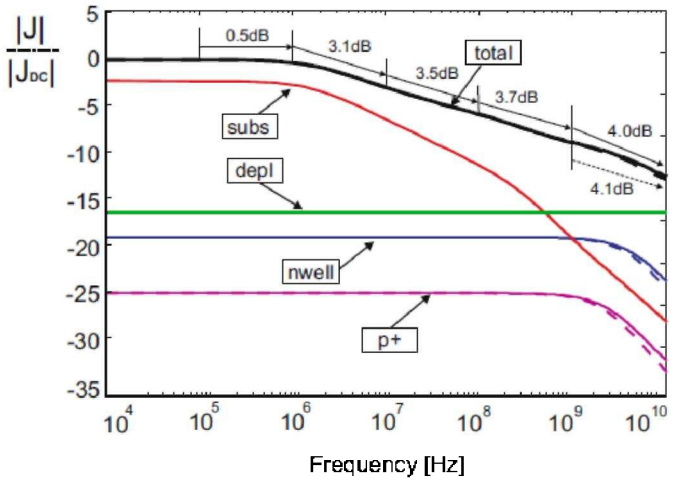


Figure 3.22: The response of p+/nwell/p-substrate photodiode with lowresistance substrate in an adjoined-wells technology: 2 µm (solid lines) and 10 µm nwell size (dashed lines) for λ = 850 nm

The bandwidth of this photodiode is higher than the nwell/p-substrate photodiode, but the responsivity is lower. That means that the photocurrent will be lower and the circuit connected to amplify the current has objectives more difficult to reach.

3.6. Scope and limitations of CMOS photodiodes

This section discuses CMOS photodiodes considering the wavelength range, bandwidth and the impedance needed to have a good impedance match to the amplifier.

3.6.1. Wavelength limitations

CMOS photodiodes work when the incident light has a wavelength between 400nm to 1µm. This range includes the visible spectrum (400nm-700nm) and part of the near infrared spectrum (700nm-2.5µm).

CMOS photodiodes fit very well for APS and others applications related to image capture and digital communications. Some of these applications are listed below.

- 10 Gigabit/sec fiber Ethernet: λ=850nm.
- CD players and recorders: λ=750nm.
- DVD players and recorders: λ=650nm.
- DVD – blue ray disc: λ=400nm.

3.6.2. Bandwidth and responsivity comparison

A nwell/p-substrate and a p+/nwell/p-substrate photodiode are compared. For comparison, the wavelength used was λ=850nm.

The Table 3.2 and Table 3.3 show the important parameters for nwell/p-substrate and P+/nwell/p-substrate of all variants.

The responsivity is normalized with respect of the responsivity of the low resistance in all the cases. The nwell/p-substrate with high resistance has the best responsivity.

The results can demonstrate that the second photodiode (p+/nwell/p-substrate) is much better than the first one (nwell/p-substrate) in terms of bandwidth. Note that the cut-off frequency is higher for low resistance substrate.

Table 3.2: Cut-off frequency and responsivity for nwell/p-substrate photodiode.

Nwell/p-substrate		Separated wells		Adjoined wells	
		Ly= 2 µm	Ly = 10µm	Ly= 2 µm	Ly = 10µm
High resistance	Cut-off frequency	1MHz	1MHz	0.6MHz	0.6MHz
	Average roll-off/dec	4.6	4.9	4.3	4.8
	Responsivity	3dB	3dB	3dB	3dB
Low resistance	Cut-off frequency	1.4MHz	1.4MHz	1MHz	1MHz
	Average roll-off/dec	3.9	4.2	3.9	4.4
	Responsivity	0dB	0dB	0dB	0dB

Table 3.3: Cut-off frequency and responsivity for p+/nwell/p-substrate photodiode.

P+/Nwell/p-substrate		Separated wells		Adjoined wells	
		Ly= 2 µm	Ly = 10µm	Ly= 2 µm	Ly = 10µm
High resistance	Cut-off frequency	1.6MHz	1.6MHz	1.2MHz	1.2MHz
	Average roll-off/dec	3.9	3.9	3.9	4
	Responsivity	3dB	3dB	3dB	3dB
Low resistance	Cut-off frequency	2MHz	2MHz	1.8MHz	1.8MHz
	Average roll-off/dec	3.3	3.3	3.1	3.15
	Responsivity	0dB	0dB	0dB	0dB

The next list shows the different photodiodes in order of their speed starting from the fastest one.

1. P+/nwell/p-substrate, separated wells, low resistance
2. P+/nwell/p-substrate, adjoined wells, low resistance
3. P+/nwell/p-substrate, separated wells, high resistance
4. Nwell/p-substrate, separated wells, low resistance
5. P+/nwell/p-substrate, adjoined wells, high resistance
6. Nwell/p-substrate, adjoined wells, low resistance
7. Nwell/p-substrate, separated wells, high resistance
8. Nwell/p-substrate, adjoined wells, high resistance

A spatially modulated photodiode can be designed (3). With this technique, is possible to have a nwell/p-substrate photodiode as fast as a p+/nwell/p-substrate one sacrificing responsivity.

To analyze the responsivity, it can be seen as a function of the frequency using the following equation (8).

$$resp(f_{ref}) = resp(0)\left(\frac{f_{cut-off}}{fref}\right)^{\frac{roll-off}{-\frac{20dB}{dec}}} \tag{3.34}$$

This is valid only for frequencies higher than the cut-off frequency.

3.6.3. Parasites comparison

The input impedance of the amplifier that is connected to the photodiode can be calculated from the parasites of the photodiode.

The parasite that influences more in the input impedance is the parasitic capacitance. This capacitance can be extracted from the photodiode design.

Once the capacitance is obtained, the input impedance can be calculated as a function of the cut-off frequency desire.

$$R_L = \frac{1}{2\pi C_j f_c} \tag{3.35}$$

The Table 3.4 shows the parasitic capacitance and the in impedance that has to be designed by the amplifier to reach 3GHz bandwidth.

Table 3.4: Parasitic capacitance and in impedance for different photodiodes.

		Separated wells		Adjoined wells	
		Ly= 2 µm	Ly = 10µm	Ly= 2 µm	Ly = 10µm
Nwell/p-substrate	Parasitic capacitance	0.28pf	0.27pf	1.6pf	0.62pF
	Input impedance	189Ω	196Ω	33Ω	85Ω
P+/Nwell/p-substrate	Parasitic capacitance	2pf	1.8pf	3.6pF	2.2pF
	Input impedance	26Ω	29Ω	15Ω	24Ω

To illustrate the use of the last table, the Figure 3.23 shows a photodiode equivalent circuit (14).

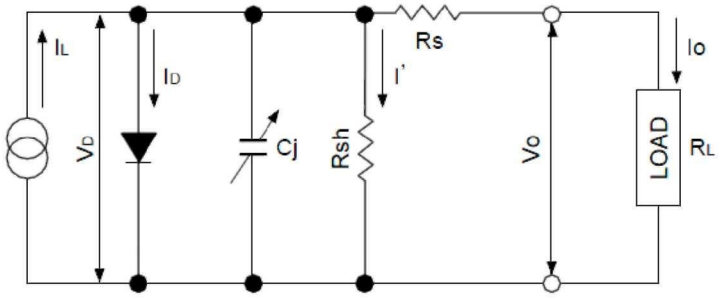


Figure 3.23: Photodiode equivalent circuit

The parasitic capacitances and the input impedance shown in the Table 3.4 are C_j and R_L of the equivalent circuit. The R_{sh} and R_s resistance are parasites that can be extracted from the photodiode layout.

Chapter 4

Simulation and design of an optoelectronic interface

The first part of this chapter shows the three designed designed: p+/nwell, nwell/p-substrate, n+/p-substrate. A spatially modulated technique was applied to the three photodiodes. Moreover, in order to fabricate the integrated circuit, the ring pad was included too.

The second part of this chapter shows the designed high bandwidth amplifier. The amplifier consists on five blocks: Transimpedance amplifier (TIA), Inductive Peaking, CMOS Inverter, Source degeneration and CMOS Inverter Amplifier.

4.1. P+/nwell photodiode design in a 0.35µm CMOS technology

This section shows the p+/nwell design. The design was a replica of the photodiode described in (2) but with the technology advisable here. The pwell could not be including in the design because of the technology. Instead of using the pwell layer, it is using the substrate. Figure 4.1 shows the design of the p+/nwell photodiode. The size of the photodiode is around 148µmx148µm.

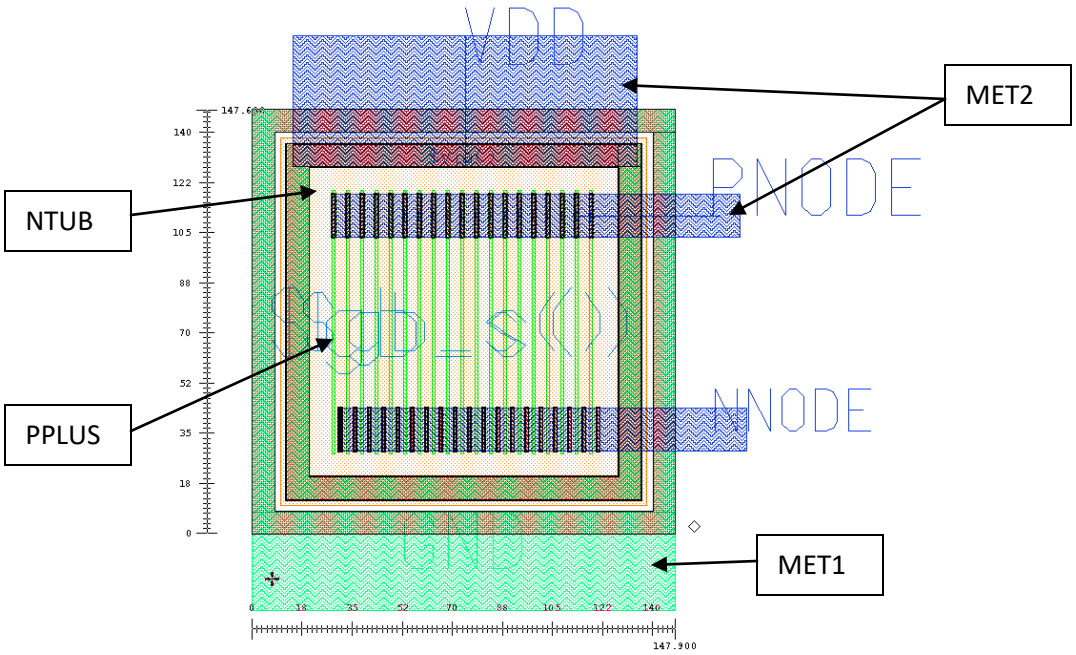
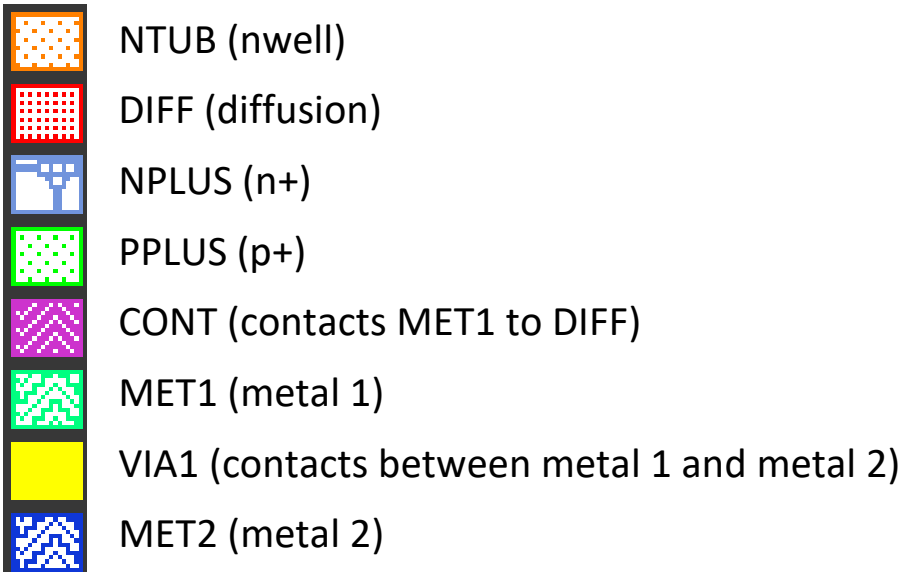


Figure 4.1: P+/nwell photodiode.

The layers used in this design are:



4.1.1. Designed blocks

The designed blocks are designs advisable in the technology library. Actually, these designs can be seen as the "union" of specific layers in a specific form to warranty the success of the Design Rule Check (DRC) test. For example, the via pdm1 has four layers: PPLUS, MET1, CONT and DIFF.

For the design of the p+/nwell photodiode, four designed blocks were used:

- Via: pdm1 (via from p+ to metal 1)
  - PPLUS
  - MET1
  - CONT
  - DIFF
- Via: m1m2 (via from metal 1 to metal 2)
  - MET1
  - MET2
  - VIA1
- Guard Band: pdsub (guard band with p+)
  - PPLUS
  - CONT
  - MET1
  - DIFF
- Guard Band: ndnwell (guard band with n+ and nwell)
  - NTUB
  - NPLUS
  - CONT
  - DIFF
  - MET1

4.1.2. Node designs of the p+/nwell photodiode

To make the correct node designs, is important to visualize the p-node (PNODE) and the n-node (NNODE) of the photodiode. For this photodiode, the signal of the PNODE is taken from the p+ structure. The signal of the NNODE is taken from the nwell.

The first node to design is the PPNODE. Figure 4.2 shows the p+ fingers with a via to metal 1. The others layers were occulted except NTUB.

The size of the fingers is 92µmx1µm. The width of the via is 15µm.

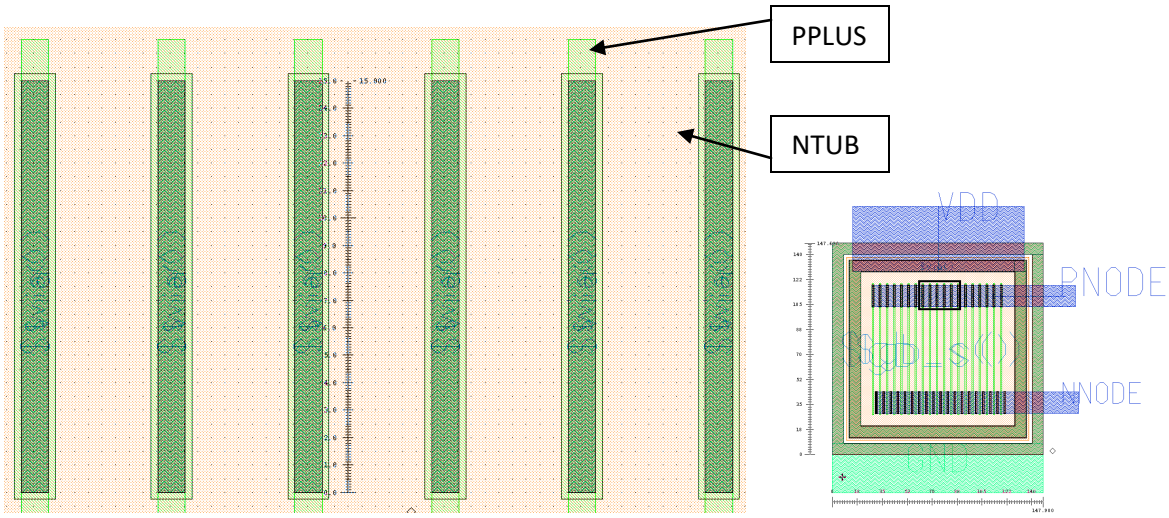


Figure 4.2: P+ fingers of p+/nwell photodiode.

To have the signal in metal 2, is necessary put a via from metal 1 to metal 2 (via: ,1m2). Figure 4.3 shows the PNODE with all the layers.

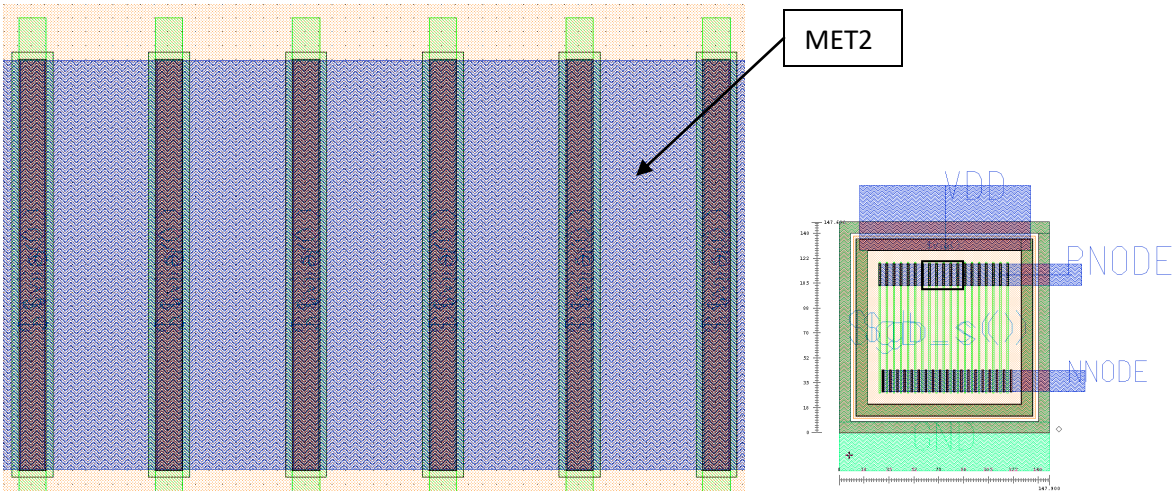


Figure 4.3: Pnode connection of p+/nwell photodiode.

The procedure to design the PNODE is:

1. Create a p+ finger and copy many times as wanted. This photodiode has 19 p+ fingers.
2. Create a via from p+ to metal 1 (via:pdm1) and copy it.
3. Create a via from metal 1 to metal 2 (via:m1m2) and copy it.

Create a NTUB rectangle with sizes higher than the p+ fingers structure. The NTUB rectangle can be designed after or before the PNODE, in this case was designed before. To obtain the signal from the nwell, this step has to be done.

To obtain the signal from the nwell, another designed block was used. A Guard Band of ndnwell is used to extract the signal to metal 1. This type of Band Guard is commonly used to keep the structure inside of it out of noise.

Once the signal is in metal 1, a via from metal 1 to metal 2 is used again. Figure 4.4 shows the NNODE connection of the p+/nwell photodiode. Note that the p+ fingers do not have connection to metal 2.

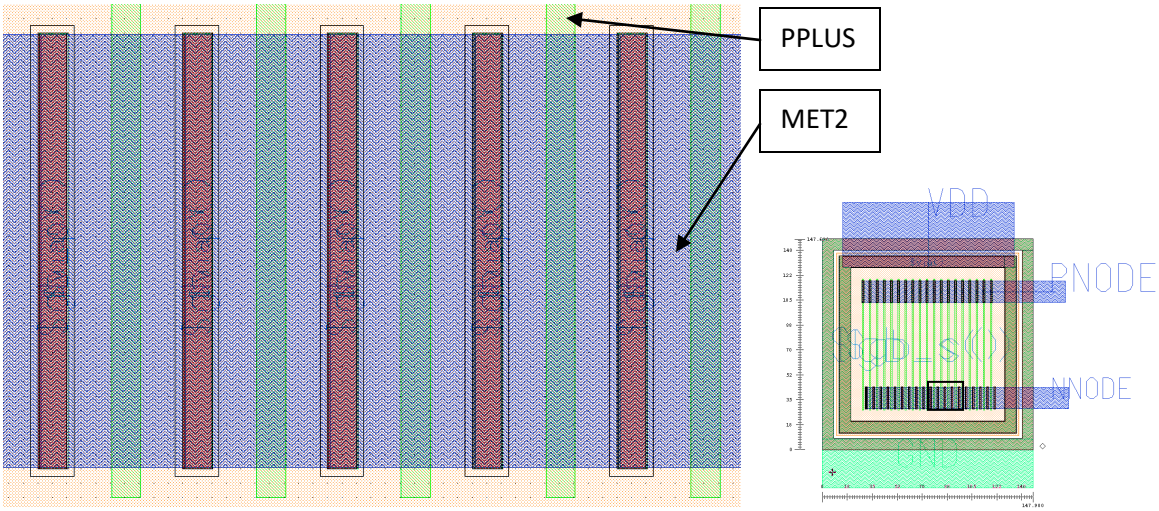


Figure 4.4: Nnode connection of p+/nwell photodiode.

The procedure to design the NNODE is the same as the PNODE only with one difference. Instead of using a via from p+ to metal 1, a guard band is used to take the signal to metal 1.

4.1.3. Guard bands design

Two guard band rings are used to keep the photodiode out of noise. The guard bands used was described before.

The type of the internal ring guard band is ndnwell and the external is pdsub. Figure 4.5 shows the two guard bands.

The internal guard band has to be connected to VDD and the external one to GROUND. To make the connection to VDD a via from metal 1 to metal 2 was used. It is necessary because both guard bands has metal 1. Figure 4.6 shows the connection of the internal ring to VDD.

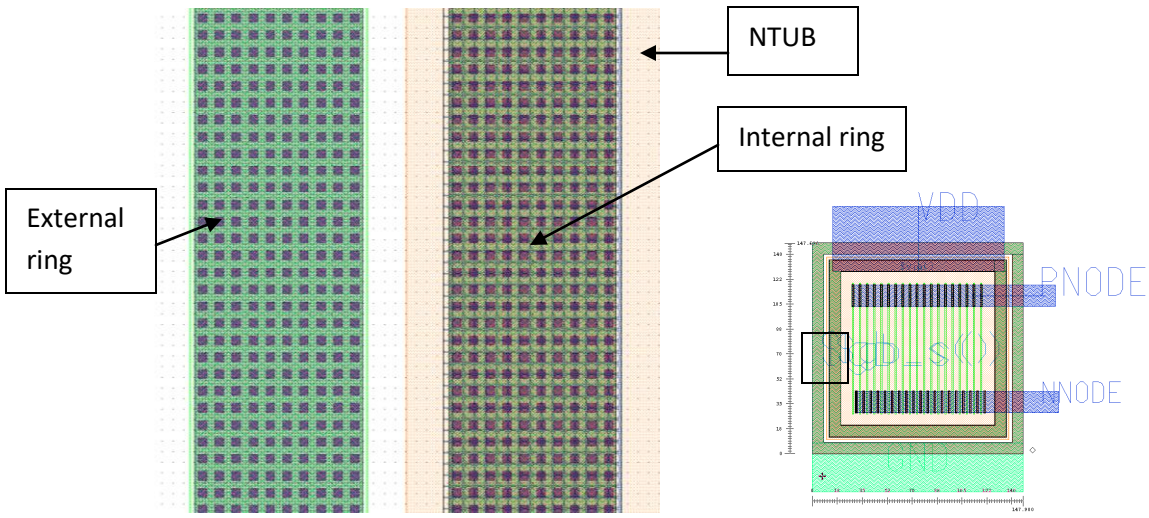


Figure 4.5: Guard bands of p+/nwell photodiode.

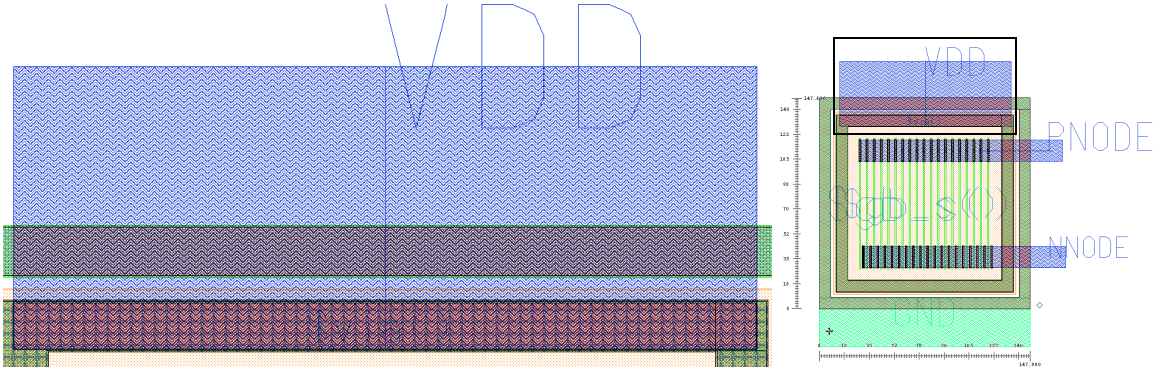


Figure 4.6: Internal ring connection.

4.2. Nwell/p-substrate photodiode design

This section shows the design of a nwell/p-substrate photodiode. A 0.35µm CMOS technology was used. The size of this photodiode is around 68µmx68µm. Figure 4.7 shows the entire photodiode design.

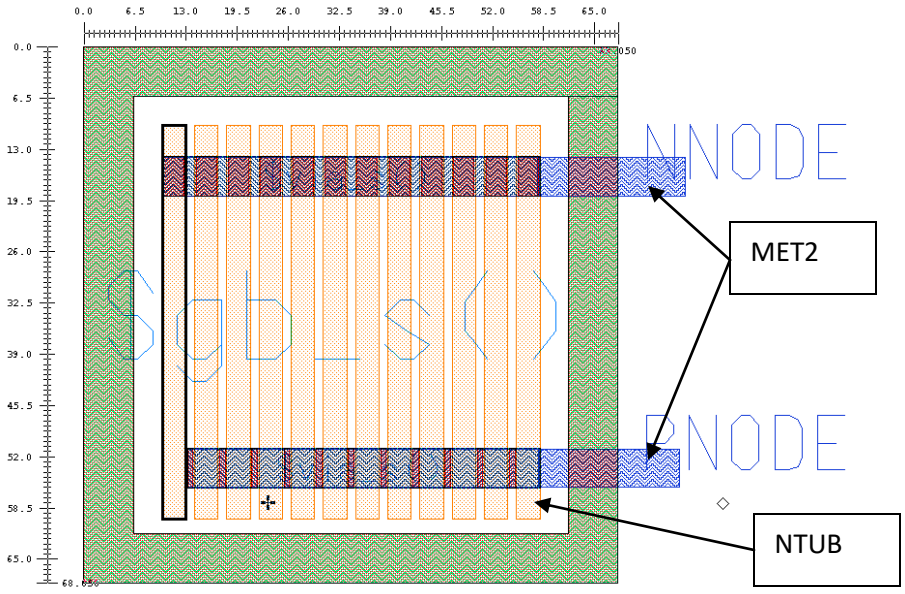


Figure 4.7: Nwell/p-substrate photodiode.

4.2.1. Node designs of the nwell/p-substrate photodiode.

The design of this photodiode was done without using designed blocks. The first block to design was de NNODE. Figure 4.8 shows the NTUB and DIFF layers of the NNODE connection.

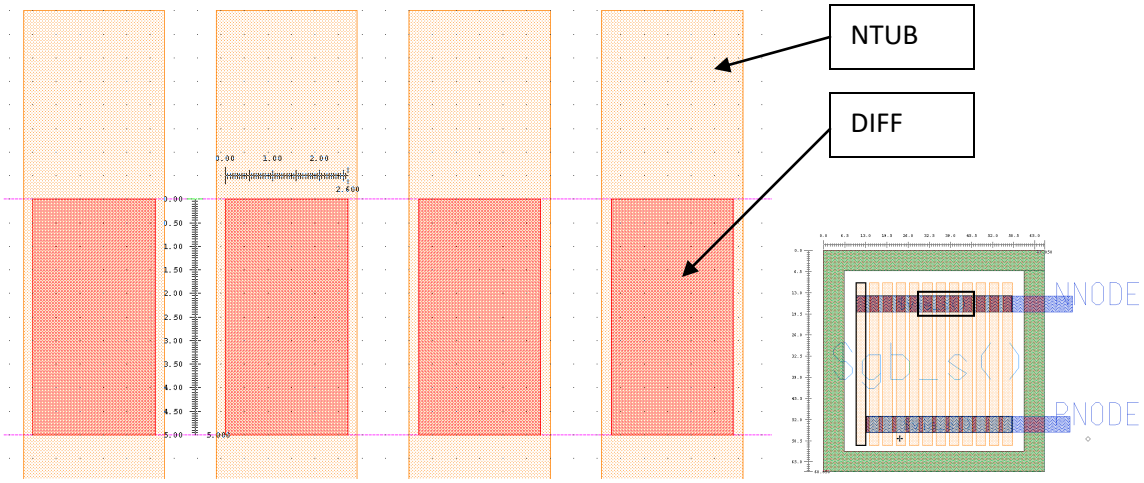


Figure 4.8: NTUB+DIFF layers of the Nnode connection.

The size of the DIFF rectangles is 2.6µmx5µm. To pass the DRC, the DIFF area has to be inside the NTUB.

Figure 4.9 shows the NTUB, DIFF and CONT layers of the NNODE connection. To pass the DRC, the size of the contacts has to be 0.4µmx0.4µm. The contacts are used to connect the Nwell to metal 1.

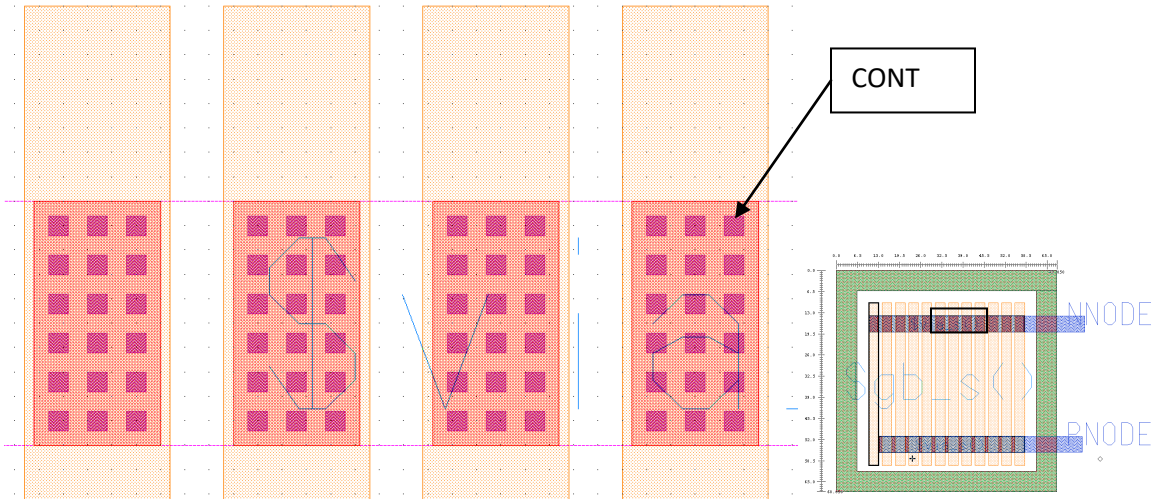


Figure 4.9: NTUB+DIFF+CONT layers of the Nnode connection.

Figure 4.10 shows the NTUB, DIFF, CONT and MET1 layers of the NNODE connection.

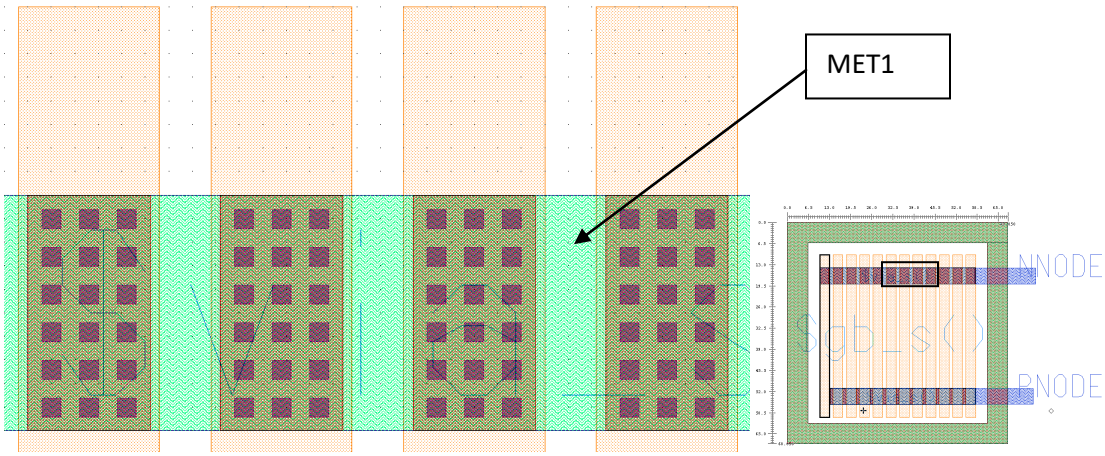


Figure 4.10: NTUB+DIFF+CONT+MET1 layers of the Nnode connection.

After putting the metal1 layer, a via from metal 1 to metal 2 was used. Figure 4.11 shows the NNODE connection with all the layers.

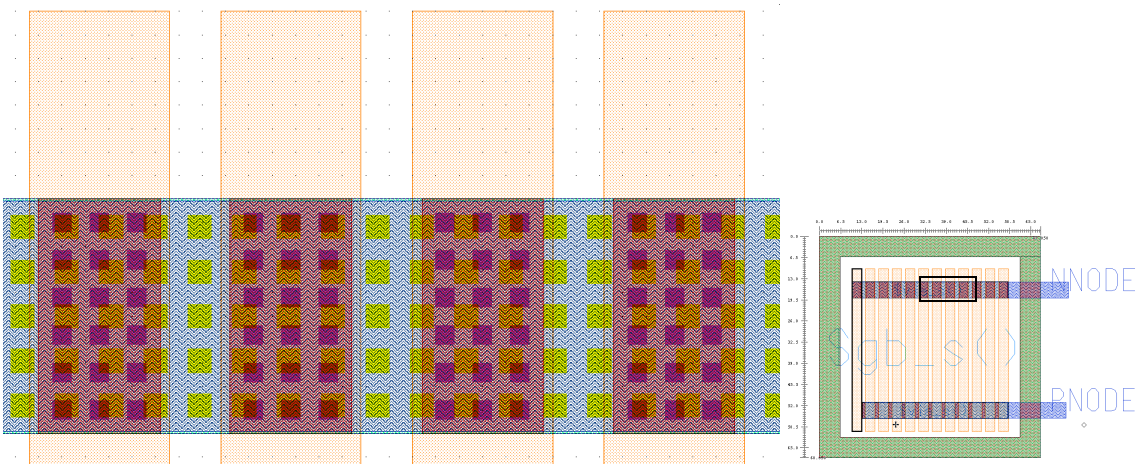


Figure 4.11: NNODE connection of nwell/p-substrate.

The design of the PNODE needs the DIFF, CONT and MET1 layers. Also a via from metal 1 to metal 2 is needed.

Figure 4.12 shows the DIFF and CONT layers of the PNODE.

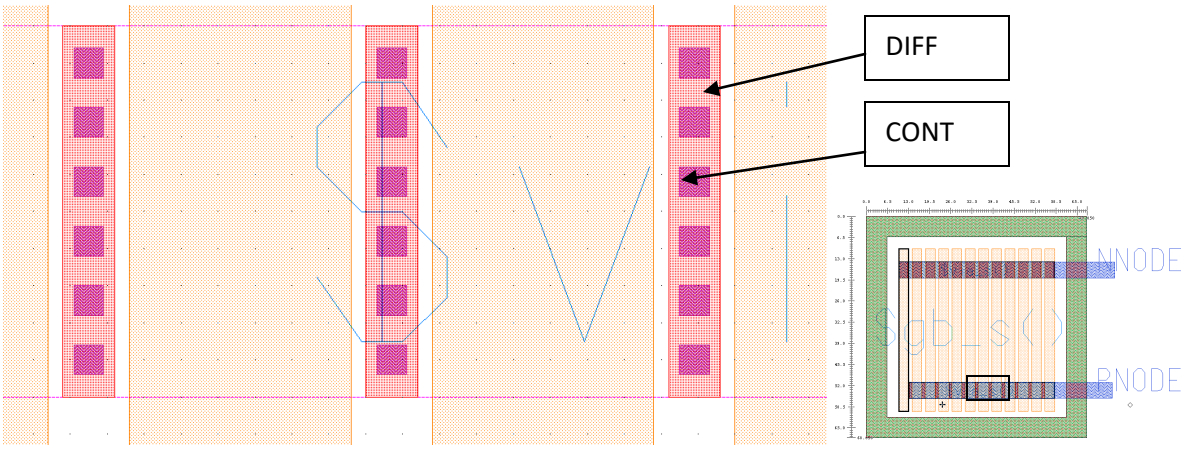


Figure 4.12: Pnode connection of nwell/p-substrate.

Only one guard band was designed for this photodiode to avoid noise. This guard band is connected to ground.

4.3. N+/p-substrate photodiode design

The procedure design of this kind of photodiode is the same as the nwell/p-substrate photodiode. Two simple changes were made. Figure 4.13 shows the n+/p-substrate photodiode.

- Instead of using the NTUB layer to make the fingers, I used the NPLUS layer.

- Instead of making the way the NNODE by putting the DIFF and CONT layers, I used a designed block. The one needed was a VIA from n+ to metal 1 (VIA: ndm1)

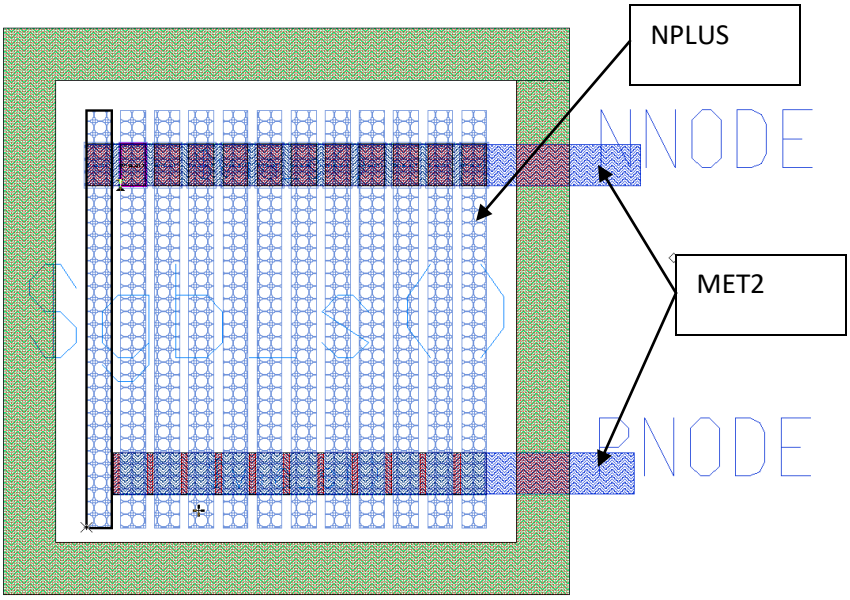


Figure 4.13: N+/p-substrate photodiode.

4.4. Spatially modulated photodiode designs

Once the nwell/p-substrate and the n+/p-substrate were designed, a metal 3 fingers were added to obtain the effect described in (3). Figure 4.14 and Figure 4.15 show those designs.

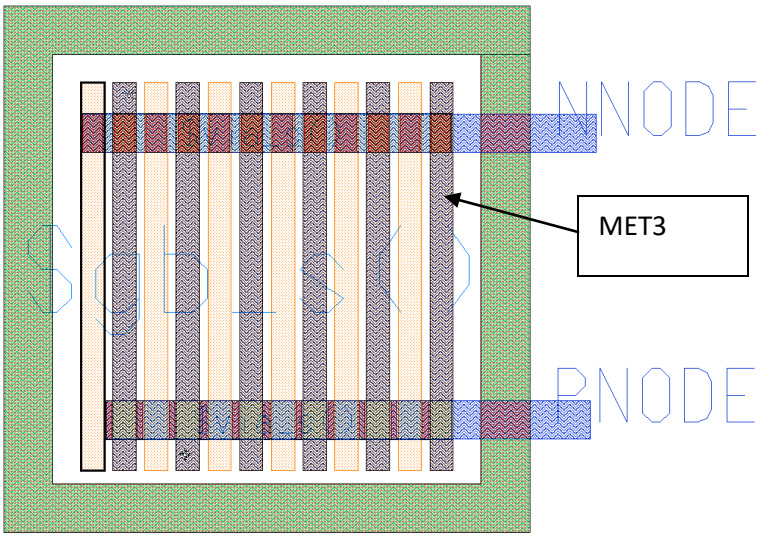


Figure 4.14: A Nwell/P-substrate spatially modulated photodiode in 0.35µm CMOS technology.

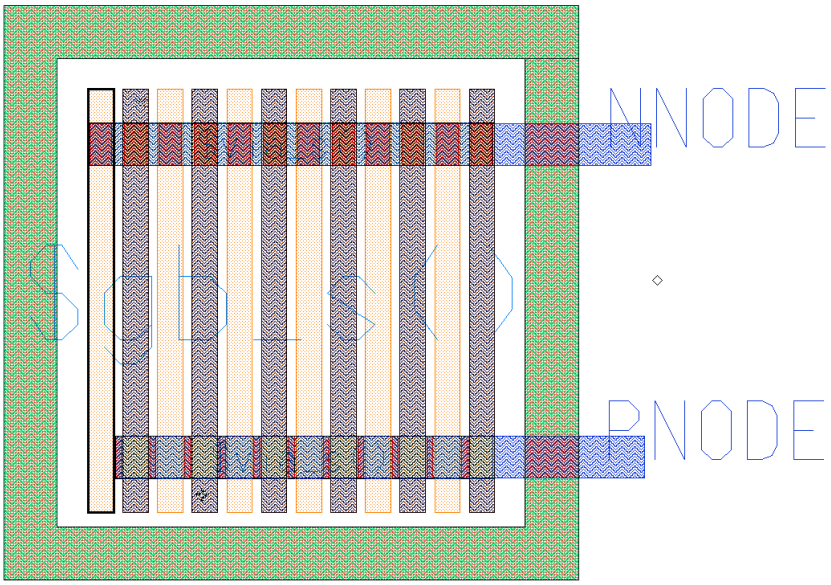


Figure 4.15: A N+/P-substrate spatially modulated photodiode in 0.35µm CMOS technology.

4.5. Ring design

Once the layout design was made, the next block to design is the ring. This is essential to do in order to fabricate an integrated circuit. The ring has the pads needed to capture the signal from the outside.

The designer can see the ring as an external design that doesn't depends on the circuits or elements designed before, but this is not truth. The size of the ring, the numbers of pads, and the types of the pads depends on the circuit design.

But once the designer knows all those things, the ring can be designed separately from the circuit. I decided to design three different photodiodes and them in the same integrated circuit. The three photodiodes are a p+/nwell, n+/p-substrate and nwell/p-substrate.

For the first one, two outputs terminal (NNODE and PNODE) and two others for the band guards rings are needed. The last two are the voltage and ground terminals.

The second one and the third one have two terminal each other (NNODE and PNODE again) and the just ground terminal is needed for the band guard ring.

The ring, in this case, has to have 6 outputs terminal, one voltage terminal and one ground terminal. With this in mind and considering the size of the three photodiodes, the ring was designed. The Figure 4.16 shows the ring design made for the three photodiodes.

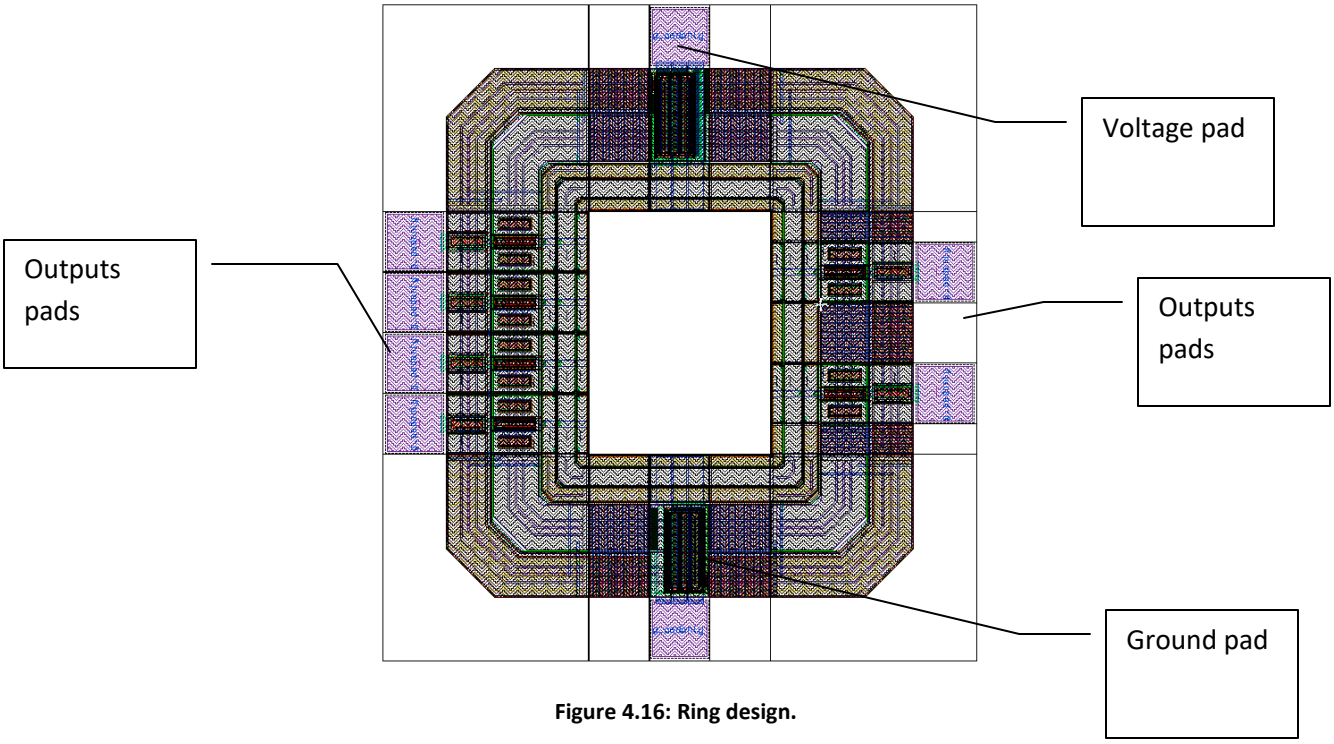


Figure 4.16: Ring design.

All the pads are designed blocks and they can be found in the technology libraries. For the technology used, those pads are called as follow.

- AVDD3ALLP
- AGND3ALLP
- APRIOP

Notice that the ring has others designed blocks to encapsulate all the circuit. The others designed blocks are called:

- CORNERP
- PERI_SPACER_50_P
- PERI_SPACER_100_P

Once the ring and the desire photodiodes were designed, it can easily incorporate both circuits into a third one. This is very helpfully for the designer for the design rule check revision. The Figure 4.17 shows the entire circuit with the ring designed.

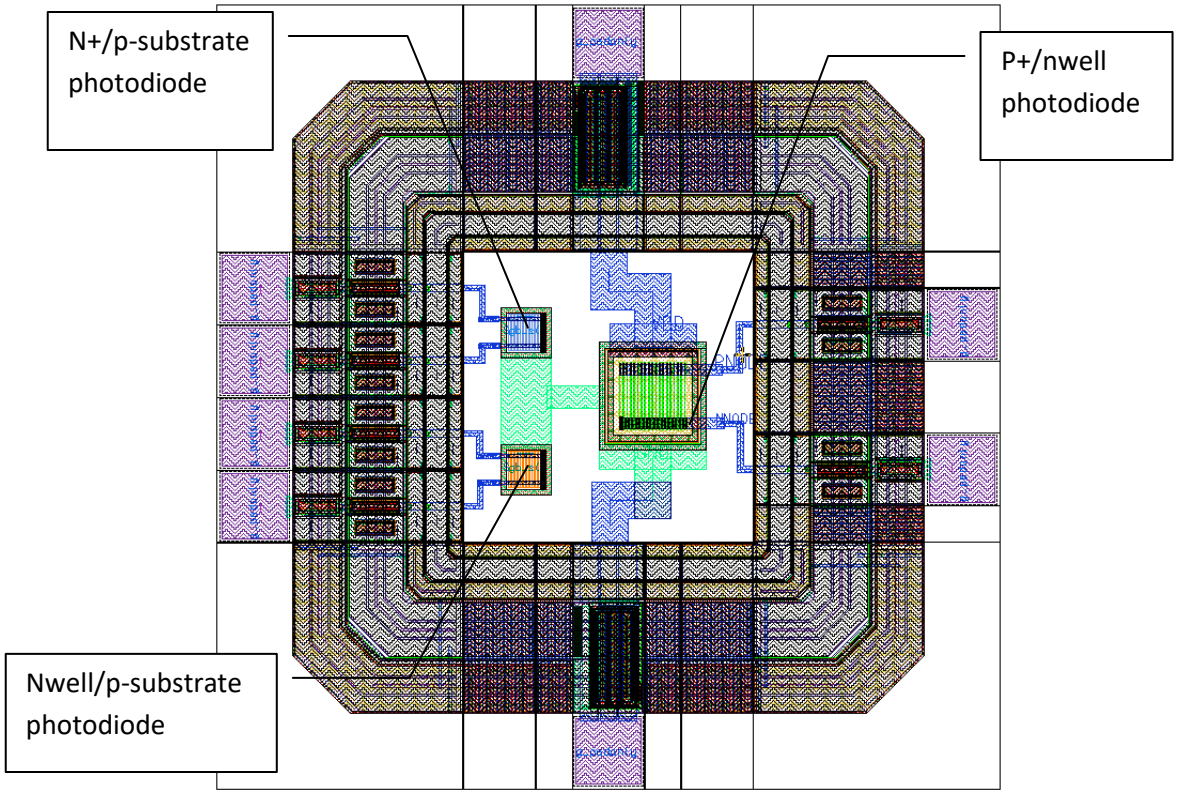


Figure 4.17: Photodiodes with ring.

4.6. High bandwidth amplifier design

Figure 4.18 shows the block diagram of the proposal amplifier. This design offered a great bandwidth but the stability is not good because of the lack of a closed-loop system. This system was designed using a 0.35µm CMOS Technology.

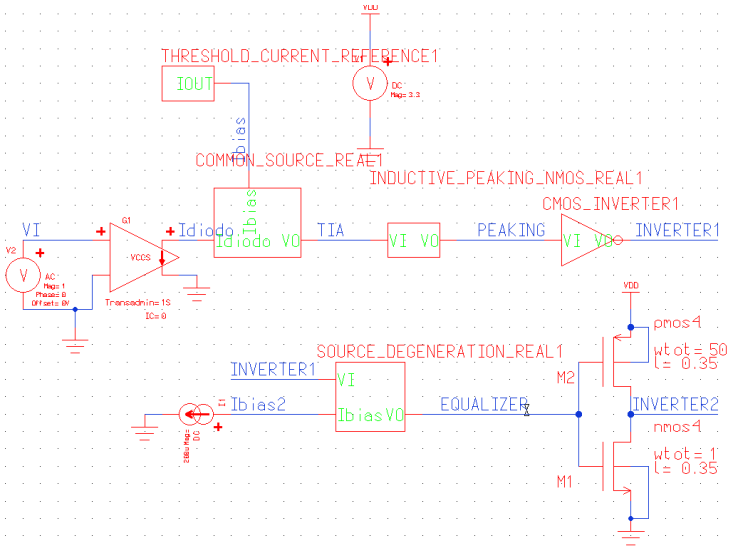


Figure 4.18: Block diagram of a high bandwidth amplifier.

The blocks of the amplifier are:

- VCCS (Voltage controller, current source).
- COMMON_SOURCE_REAL1.
- THRESHOLD_CURRENT_REFERENCE1.
- INDUCTIVE_PEAKING_NMOS_REAL1.
- CMOS_INVERTER1.
- SOURCE_DEGENERATION_REAL1.

The current range was obtained from the Figure 3.18. The minimum current is 2μA and the maximum current is 40μA. The VCCS is used to simulate the photocurrent. The transadmitance was set at 1S (1 siemens) in order to convert a voltage source into a current level. The others blocks are explained in more details later.

Three kinds of analysis were realized using this circuit, a dc analysis, ac analysis and a transient analysis.

4.6.1. Transimpedance amplifier

The goal of the TIA is to change the current level into a voltage level. The transfer function ($\frac{V_{out}}{I_{in}}$) of this block has resistive dimensions (Ω), for that reason they are called "transimpendance amplifiers". The Figure shows the schematic representation and idealized model of these amplifiers.

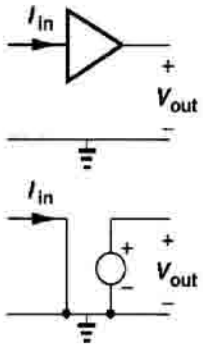


Figure 4.20: Schematic representation and ideal model of the transimpedance amplifier.

This block can be done with a few transistors and resistors. Figure 4.21 and Figure 4.22 show two designs of a TIA(15).

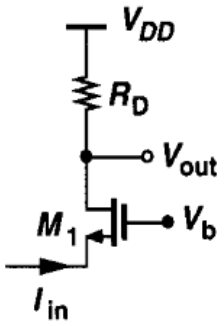


Figure 4.21: Common-Gate circuit as a transimpedance amplifier

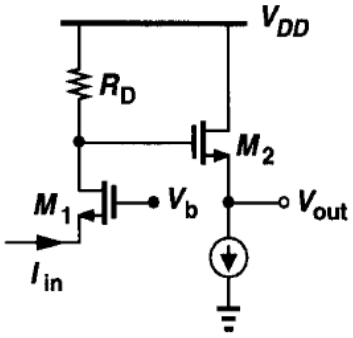


Figure 4.22: Improved circuit for transimpedance amplifier

Figure 4.23 shows a common source circuit using as a TIA. This design is much simpler; only consist in a transistor, a resistor and a current source.

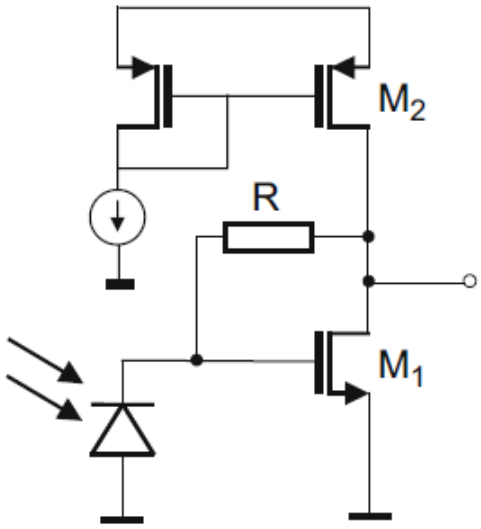


Figure 4.23: Common source as a transimpedance amplifier

$$\frac{V_{out}}{I_{in}} = R_o \frac{1 - Rg_{m1}}{1 + R_0 g_{m1}} \approx -R \tag{4.1}$$

$$R_{in} = \frac{R + R_o}{1 + R_o g_{m1}} \tag{4.2}$$

$$R_{out} = \frac{R_o}{1 + R_o g_{m1}} \approx \frac{1}{g_{m1}} \tag{4.3}$$

R_o is the combined output resistance of M1 and M2.

$$R_o = \frac{1}{g_{m1} + g_{m2}} \tag{4.4}$$

Common source topology for a TIA is used in the high bandwidth amplifier. Two considerations were made to select the R value of this amplifier, the output swing voltage and the highest expected photocurrent. Figure 4.24 shows the circuit capture of the TIA.

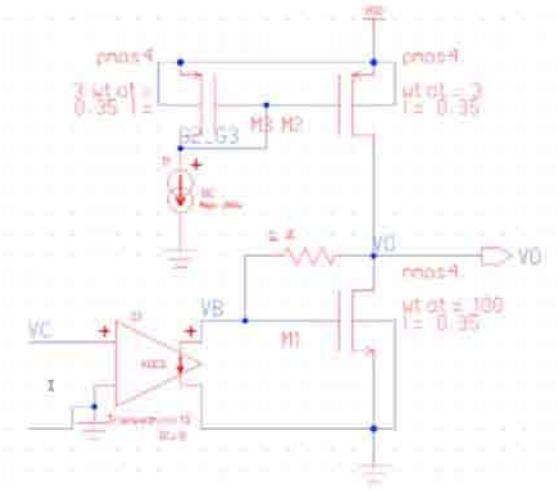


Figure 4.24: TIA design.

The output swing voltage wants to be equal to 100mV and the highest expected current is 40µA.

$$R = \frac{100mV}{40\mu A} = 2500\Omega$$

The dimensions of the transistors and the bias current were select to have good input impedance.

- $(W/L)_1 = \frac{100}{0.35}$
- $(W/L)_2 = \frac{3}{0.35}$
- $I_d = 200\mu A$

Using those parameters, the R_{in} and R_{out} are:

$$R_{in} = 167\Omega$$

$$R_{out} = 226.87\Omega$$

The simulation test proves that using a 3KΩ resistor, the output voltage swing will be 105mV. The R_{in} and R_{out} are:

$$R_{in} = 161\Omega$$

$$R_{out} = 98.23\Omega$$

4.6.2. Current source

To design the 200µA current source, a threshold current reference topology was used. Figure 4.25 shows the schematic design.

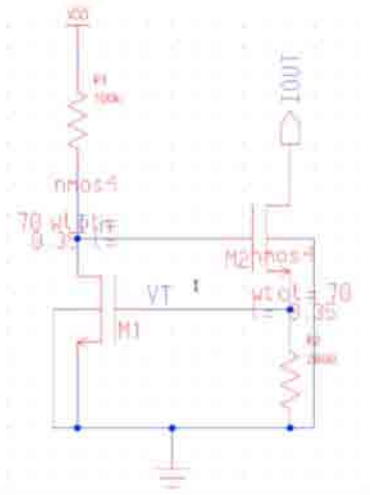


Figure 4.25: Threshold current reference.

The only design parameter in the threshold current reference is the resistor R2. The others parameters maintain the two transistors in saturation region. The R2 resistor is calculated dividing the V_T voltage by the I_{bias} current (200µA).

$$R_2 = \frac{0.45}{200\mu} = 2250\Omega$$

Simulating with that value, the current was higher than expected. For that reason, the resistor used was:

$$R_2 = 2800\Omega$$

4.6.3. Analog equalizer

The goal of this block is to compensate the photodiode frequency behavior to increase the bandwidth. A source degeneration circuit is proposed for this block. Figure 4.26 shows the schematic of the analog equalizer.

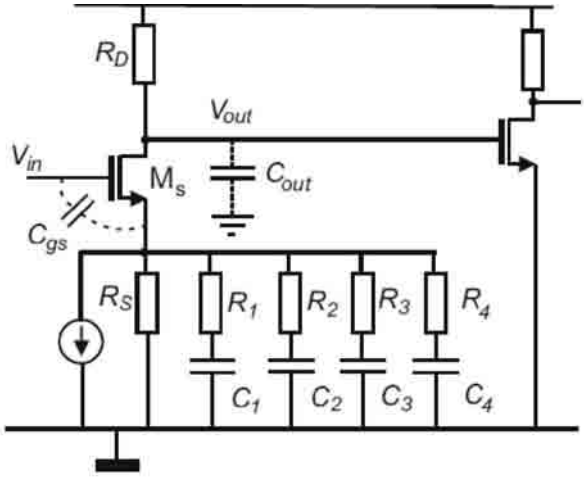


Figure 4.26: Analog equalizer.

The circuit consists in four high-pass filters. Each high-pass filter has different cut-off frequency in order to emphasize a particular bandwidth.

Making $R_D = R_s$, the resistors and capacitance can be designed as follow:

1. Define the bandwidth to be emphasized ($f_{min} - f_{max}$).
2. Define the numbers filters (N) to be designed.
3. Define the gradient in decibels (ΔdB) between each filter.
4. Find each cut-frequency, resistance and capacitance given by the following equations:

$$f_n = f_{min}\left(\frac{f_{max}}{f_{min}}\right)^{\frac{n-1}{N}} \tag{4.5}$$

$$R_n = \frac{R_D}{10^{\frac{\Delta dB.n}{20}} - 10^{\frac{\Delta dB.(n-1)}{20}}} \tag{4.6}$$

$$C_n = \frac{1}{2\pi f_n R_n}; n = 1,2..N \tag{4.7}$$

The first high-pass filter of the analog equalizer is implemented by an active inductor. Figure 4.27 shows the schematic of the inductive peaking proposed (16).

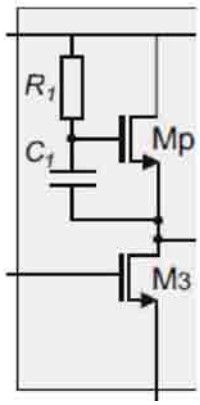


Figure 4.27: Inductive peaking schematic.

Figure 4.28 shows the schematic capture of the inductive peaking.

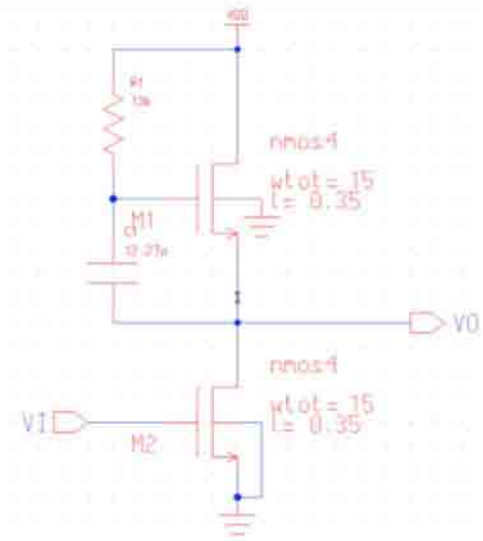


Figure 4.28: Inductive peaking design.

Using the procedure explained the resistor and capacitance values are shown in the Table 4.1.

$$\Delta dB = 3.75$$

$$N = 4$$

$$f_{max} = 1GHz$$

$$f_{min} = 1MHz$$

$$R_D = 7K\Omega$$

Table 4.1: Capacitances and resistances of the source degeneration circuit.

n	$R_n(\Omega)$	$f_n(Hz)$	$C_n(pF)$
1	12964.727	1,000,000	12.2759965
2	8419.05556	5,623,413	3.36168299
3	5467.18004	31,622,777	0.92056987
4	3550.28629	177,827,941	0.25209066

All the resistance and capacitance values were found. To obtain the size of the transistors, simulations of the previous block and others considerations was realized.

The first step is to know the input voltage range. The voltage range was obtained by simulating the common source circuit explained before.

$$V_{TIA} = 657mV - 762mV$$

The voltage to calculate the size of the transistor M2 is the average voltage expected at the input (710mV). With that value, the average current expected can be calculated applying the saturated current equation.

$$\bar{I_D} = \frac{K_N}{2}\left(\frac{W}{L}\right)_2 (\overline{V_{TIA}} - 0.45)^2$$

Using $\left(\frac{W}{L}\right)_2 = \frac{15\mu}{0.35\mu}$, the current will be 246μA. That current is used to calculate the channel conductance parameter of the transistor M1, g_{m1}.

$$g_{m1} = \sqrt{2K_N\left(\frac{W}{L}\right)_1 \bar{I_D}}$$

The value of g_{m1} has one restriction because of the inductive peaking behavior. As is explained in (16), in order to have an inductive behavior, the pole of the transfer function has to be higher than the zero.

$$Z_{out} = \frac{1}{g_{m1}}\frac{1 + sR_1C_1}{1 + s\frac{1}{g_{m1}}C_1}$$

$$\frac{g_{m1}}{C_1} > \frac{1}{R_1C_1}$$

$$g_{m1} > \frac{1}{R_1}$$

$$g_{m1} > 77.13\mu S$$

Where the values of R_1 and C_1 is taken from the first row of the Table 4.1. In fact, the capacitance C_1has to be added to capacitance $C_{gs}$of the transistor M1 but this capacitance is much smaller than C_1, for that reason is neglected.

Using $\left(\frac{W}{L}\right)_1 = \frac{15\mu}{0.35\mu}$, the channel conductance will give 1.9mS. The size of the transistor M1 could be much lower, but with this value the output swing reach almost 100mV, the same as the input.

To maintain the same sloop relation, a CMOS inverter was introduce between the inductive peaking and the source degeneration. Figure 4.29 shows the schematic capture of the CMOS inverter used.

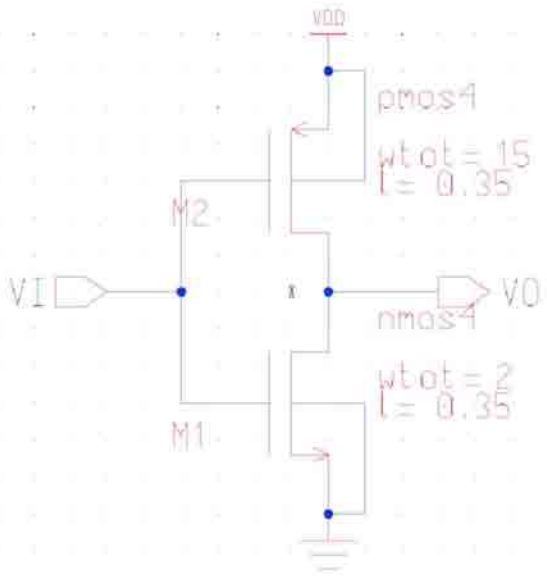


Figure 4.29: CMOS inverter design.

The objective of this block is to invert the signal because the next block needs other range of voltage.

The input swing voltage of this block is from 2.23V to 2.14V. To invert the signal and have a good output swing is necessary that the switching voltage would be high (17).

$$V_s = \frac{3.3 - 0.4 + 0.45\chi}{1 + \chi}$$

$$\chi = \sqrt{\frac{W_N E_{CP}}{W_P E_{CN}}} = \sqrt{\frac{24x10^4 W_N}{6x10^4 W_P}}$$

Where E_C is the critical electric field of the NMOS or PMOS and are constants according to the technology used. Using $W_N = 2$ and $W_P = 15$, the switching voltage is 1.86V, near from the input voltage range. To certify that the behavior wished is realized by the CMOS inverter, it was necessary to simulate and to prove some sizes of the transistors.

To find the size of the transistor, it was necessary simulate the previous blocks. Figure 4.30 shows the schematic capture of the source degeneration.

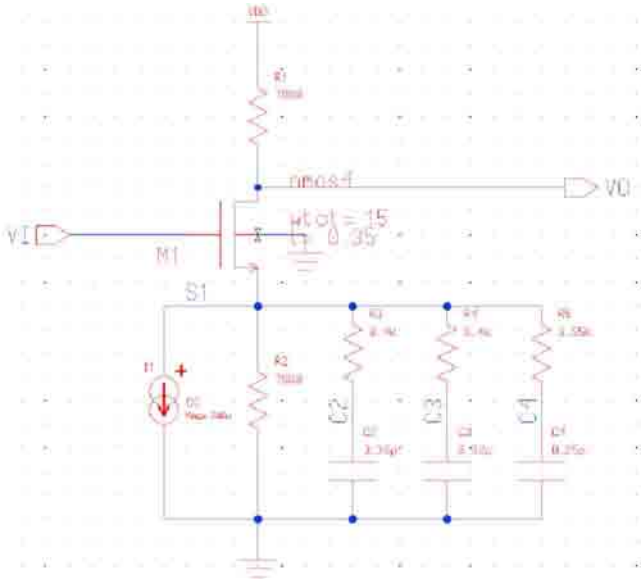


Figure 4.30: Source degeneration circuit.

This block can be seen as a resistive load inverter and the switching voltage can be calculated by equating the two currents (17)

$$\frac{K_N}{2}\left(\frac{W}{L}\right)_1 (V_S - 0.45)^2 = \frac{V_{DD} - V_S}{R_1}$$

Using $\left(\frac{W}{L}\right)_1 = \frac{15\mu}{0.35\mu}$ and $R_1 = 7000$, the switching voltage can be calculated solving the quadratic equation showed.

$$V_s = 0.765V$$

This value is low enough to get the desire behavior at the output.

4.6.4. Voltage amplifier

The second CMOS inverter is used to have at the output a non-inverter signal referring to the photocurrent. That means that until higher is the photocurrent, higher will be the voltage at the output and not vice versa. The other goal of this inverter is to have the best output swing voltage.

The procedure to design this CMOS inverter is the same as the first one. But in this one, is more critical to have the switching voltage very near to the input voltage range. The input voltage range in this case is from 2.35V to 2.26V and the switching voltage using $W_N = 1$ and $W_P = 50$ is 2.35V. The Figure 4.31 shows the schematic capture of the last CMOS inverter.

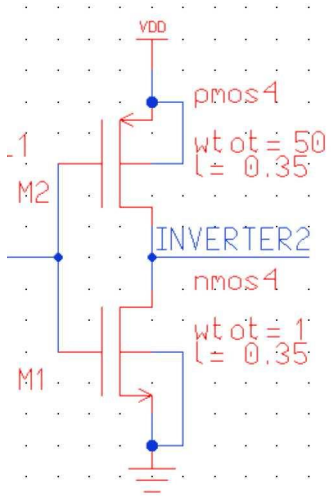


Figure 4.31: Voltage amplifier.

The Table 4.2 shows the voltages ranges and the switching voltage at the last three blocks.

Table 4.2: Voltage ranges.

Inverter1			Source degeneration		Inverter2	
Input range (V)	Vs (V)	Output range (mV)	Vs (mV)	Output range (V)	Vs (V)	Output range (V)
2.14-2.23	1.86	203-321	765	2.26-2.35	2.35	1.139-3.006

4.6.5. Simulation results

A DC analysis was realized to verifying the output swing in each block. The most important is the output of the entire system. The Figure 4.32 shows the DC analysis using a DC voltage source from 2µV to 40µV to simulate the photocurrent range.

From top to bottom of the Figure 4.32, the curves shown are:

- TIA output (TIA).
- Inductive peaking output (PEAKING).
- The first CMOS inverter output (INVERTER1).
- The source degeneration output (EQUALIZADOR).
- The second CMOS inverter output (INVERTER2).

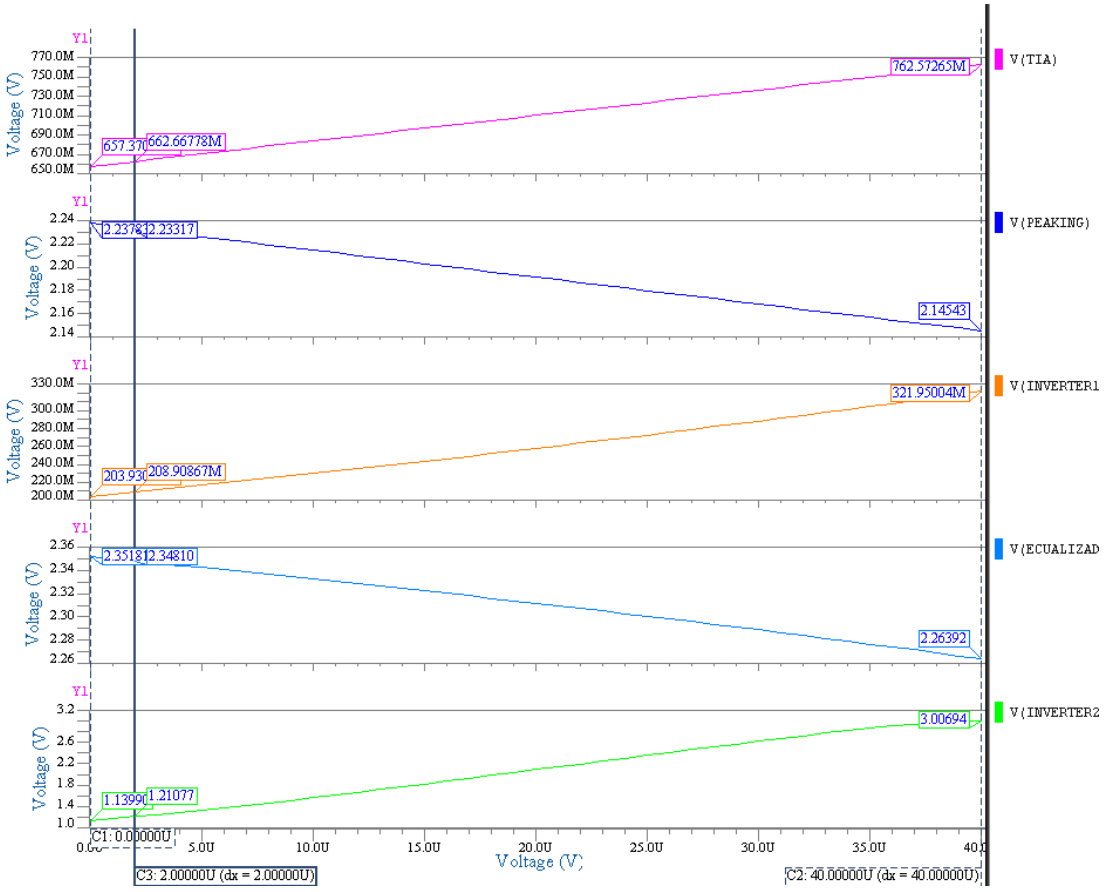


Figure 4.32: DC analysis

Three measurements are shown by each curve. The voltage when the current is 0A, 2µA and 40µA. The Table 4.3 shows these simulation tests.

Table 4.3: DC analysis results.

Input current (µA)	TIA (mV)	PEAKING (V)	INVERTER1 (mV)	EQUALIZER (V)	INVERTER2 (V)
0	657.37	2.2378	203.93	2.3518	1.1399
2	662.66	2.2331	208.90	2.3481	1.2107
40	762.57	2.1454	321.95	2.2639	3.0069

From table 4.3, the transimpedance parameter can be calculated as $47\,{}^{V}/_{mA}$.

An AC analysis was done to calculate the bandwidth of the system. In this case two curves were shown in the Figure 4.33, one is the voltage gain in decibels at the TIA output and the second one is the voltage gain at the output of the amplifier. The real gain of the system will be the subtraction of the two gains shown.

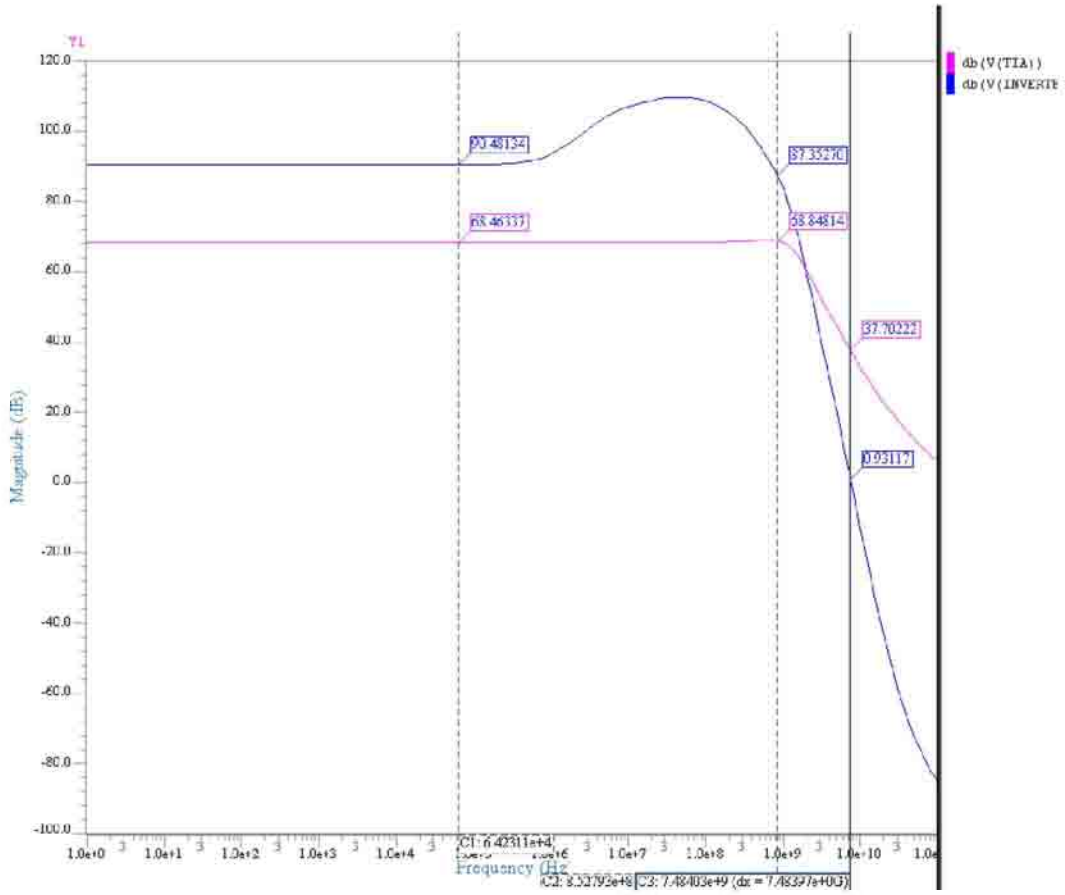


Figure 4.33: AC analysis.

A strange behavior is presented in the AC analysis seen in the output of the system (INVERTER2). That peak is done by the inductive peaking and source degeneration block. This topology explained in (8) is used because the bandwidth behavior of the photodiode.

This simulation does not have considering the frequency photodiode response. In order to have a real behavior of the entire system (photodiode and amplifier) it is necessary to find a way to estimate the frequency response.

Three measurements are important in an AC analysis, the frequency bandwidth, gain-bandwidth and the gain. From the last figure, the frequency bandwidth is 852MHz; the gain-bandwidth is around 2GHz and the gain is 22dB.

The last analysis is a transient analysis. This was done by having a voltage source changing its values at different times. The Figure 4.34 shows two curves: First, the input that changes its values from 0V to 2µV, 40µV and 21µV (mention a voltage level or current level is the same because the use of the VCCS) and second, the curve of the output of the system (INVERTER2).

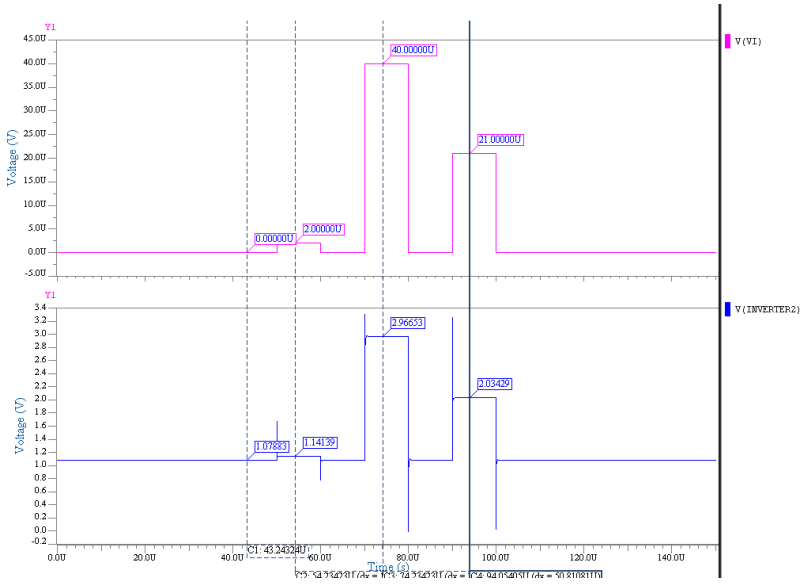


Figure 4.34: Transient analysis.

The DC values of the second curve are almost the same as illustrated Table 4.3. The characteristic transient analysis is shown by the Figure 4.35. The time needed by the output to change from 1.07V to 2.93V is 295.7ns.

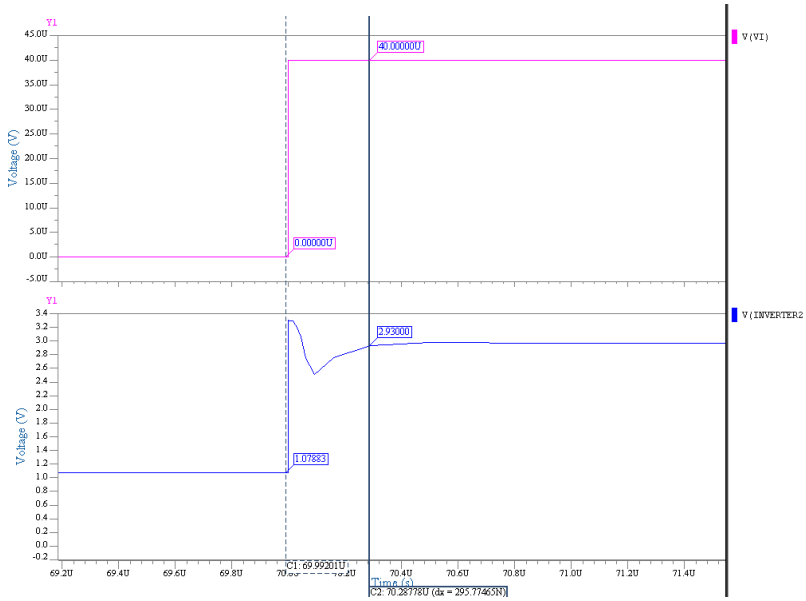


Figure 4.35: A closed view of the transient analysis.

Chapter 5

Conclusions and futures work

This thesis has been developed to support the BioMEMS research group that is working on several projects related to optoelectronic interfaces for spectrophotometers.

5.1. Conclusions

My own conclusions are listed below.

- It is possible to design CMOS photodiodes to work in the visible range and part of the NIR spectrum.
- Spatially modulated photodiodes can be implemented in CMOS technology in order to increase the bandwidth. Unfortunately, this technique reduces the responsivity.
- For the applications where the wavelength range is higher than 1µm, silicon photodiodes are not suitable. For this wavelengths range, GaAs or other special materials have to be used. These special materials are essential to monitor some physiological variables like glucose concentration.

- In this thesis, I have used 0.35µm CMOS which is a low cost technology. We can use 0.18um technologies for future works, especially if we want to incorporate digital circuits to the interface.

5.2. Future works

A list of the future research lines are:

- The characterization of the different photodiodes. This can be done in two ways.
  - Create modules using HDL (hardware description language) and incorporate them in the simulator. This strategy allows to perform a simulation of the complete system.
  - Using the PEX (Parasite extraction) module. This module allows to extract the parasite elements and to build a schematic circuit. This circuit can be used to simulate the photodiode behavior.
- A physical realization of the photodiode. Even if the amplifier is not included in the chip, the photodiodes can be fabricated and tested using external amplifiers.
- The design of a closed-loop circuit to amplify the photocurrent. Figure 5.1 shows a topology that can be used in applications where a high bandwidth circuit is not needed (18).

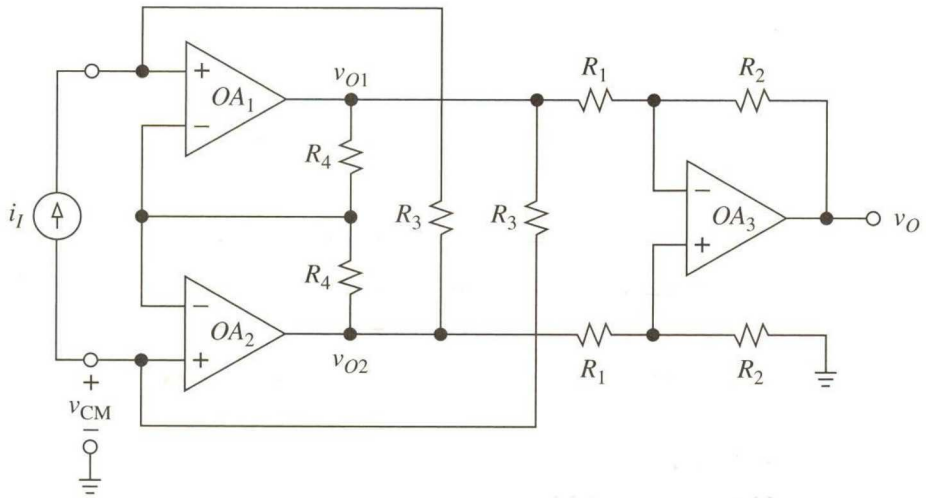


Figure 5.1: Input current instrumental amplifier.

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