INSTITUTO TECNOLÓGICO Y DE ESTUDIOS SUPERIORES DE MONTERREY

MONTERREY CAMPUS

GRADUATE PROGRAM IN MECHATRONICS AND INFORMATION TECHNOLOGIES

TECNOLÓGICO DE MONTERREY®

DESIGN OF AN ANALOG CMOS INTERFACE FOR RESONANT MICROSENSORS

THESIS

PRESENTED AS A PARTIAL FULFILLMENT OF THE REQUIREMENTS FOR THE DEGREE OF

MASTER OF SCIENCE WITH MAJOR IN ELECTRONIC ENGINEERING

(ELECTRONIC SYSTEMS)

BY

LUIS ERNESTO SARACHO MARTÍNEZ

MONTERREY, N.L., MÉXICO. MAY, 2008

INSTITUTO TECNOLÓGICO Y DE ESTUDIOS SUPERIORES DE MONTERREY

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GRADUATE PROGRAM IN MECHATRONICS AND INFORMATION TECHNOLOGIES

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A mi familia...

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DESIGN OF AN ANALOG CMOS IC INTERFACE FOR BIOMEMS SENSOR APPLICATIONS

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Instituto Tecnológico y de Estudios Superiores de Monterrey, 2008

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Abstract

The aim of this thesis is to design a CMOS analog integrated circuit for conditioning a MEMS sensor frequency signal of up to 100 *kHz,* with an amplitude up to 1 μV_P. The circuit is designed with the CMOS AMS® 0.35 μm technology process parameters.

In order to facilitate the design process, a modular methodology is used. The design starts with the requirements of the complete system, such as gain, bandwidth, power dissipation, etc., and follows with the schematic design of each individual stage.

The amplifier design is based on the synthesis of an OTA device which meets signal specifications of typical MEMS transducers for both, frequency and level voltage inputs, which are around 50 *kHz,* and 10 μV_P , respectively. Analytical and simulation results show differences of less than 10 % in the instrumentation amplifier gain, less than 5 % in the gain bandwidth approximation, and less than 7 % in the slew rate parameter for the instrumentation amplifier and the associated devices of the frecuency signal conditioning circuit designed for MEMS resonant sensors. The simulation analysis of all stages is performed in both, individual fashion and also in integrated form to verify the complete system operation of the frequency conditioning monitor circuit.

Finally, this thesis develops the layout of the circuit, following the same modular methodology, and obtaining reusable modules of the synthesized CMOS stages.

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Chapter 1

Introduction

Recent advances in complementary metal-oxide semiconductor (CMOS) processing and micromachining technologies have allowed various types of microsensors to be integrated within signal processing circuit in a single chip. The so-called *systems on chip* are increasingly used in many biomedical and chemical applications [9].

The use of microelectromechanical systems (MEMS) as sensors and microestructures offers several advantages, such as excellent mechanical properties, mature integrated circuit (IC) technology and low cost fabrication. Moreover, some emerging applications include gyroscopes, microphones, spectrometers, liquid chromatographs, bio-labs on a chip (chemical, biological and nanochemical) [10]. These systems on chip are capable of measure: tactile pressure [11], barometric pressure [12], acceleration [13], pH level [14], electrochemical concentrations [15] and ultrasonic signals [7], among other physical parameters. The magnitude of the electronic signal obtained from MEMS sensors can be of the order of 5 μV. Depending on the sensing mechanism and the signal nature as well, it could be either ac-current, dc-current, ac-voltage, or dc-voltage [14]. Therefore, on each MEMS application, there is a need for a low-power interface circuit, which serves as a bridge between the on-chip sensor and the back-end digital processor [16].

1.1 Problem Statement

The BioMEMS Research Group at Instituto Tecnológico y de Estudios Superiores de Monterrey, Campus Monterrey is developing a MEMS fully functional biosensor to monitor leukemia patients after treatment [17, 18]. The sensor mechanism is based on

the resonant behavior of silicon cantilever beams. The advantage of resonant sensors is that the frequency output is already in digital form, and hence, can be more safely transmitted from the transducer element to an electronic circuit [19]. However, the small variation generated by the sensing mechanism produces very small changes in the electronic signal [20].

Moreover, the BioMEMS Research Group is developing a multiplexed potentiostat system to convert the ionic current produced by an electrolytic reaction to a measurable signal. In order to comply with this application, a low-noise, good linearity and high sensitivity amplifier is required for developing the potentiostat microelectronic circuit [21].

This thesis develops a CMOS analog signal conditioning circuit for a low-voltage differential signal coming from resonant microsensors. The thesis defines a proper configuration for the microelectronic circuit as well as its physical layout. The process technology used is the 2-poly, 4-metal, 0.35 μm CMOS from Austriamicrosystems® (AMS) and the circuit is designed to operate at 3 V rail to rail. The design should be capable of amplifying signals of the order of 1 μV and hundreds of kHz as well.

1.2 Objectives

The general objective of this thesis is to design a CMOS circuit capable of reading and amplifying a low-voltage differential signal from a resonant sensor. The circuit will overcome noise sources in order to provide measurable signals to standard microelectronic circuits [22]. The complete system will be implemented in layout form, complying with general analog matching techniques [23], for its later integration to the projects currently in development by the BioMEMS Research Group. The specific objectives are:

- To design a CMOS signal conditioning circuit for sensing resonant beams, following a well specified methodology.
- To design the schematic diagram of the circuit by implementing the 0.35 μm process technology from AMS®.
- To design the layout of the circuit, taking advantage of general matching layout techniques for a robust physical design.

- To complete both, a functional microelectronic circuit design and a well established layout design for a two-stage CMOS operational transconductance amplifier (OTA), in order to apply this design on the signal conditioning system in the current projects of the BioMEMS Research Group.

The key contributions of this thesis are the design methodology of the CMOS circuit which can be adapted to the requirements of a specific project, and the layout design of the schematic circuit diagram, considering general matching techniques while achieving proper performance.

1.3 Previous Work

The merging of silicon microfabrication techniques with surface functionalization biochemistry offers new exciting opportunities in developing microscopic biomedical analysis devices with unique characteristics. Micromechanical transducers for chemical and biosensing applications represent one possibility.

Several biomedical applications can be foreseen, such as monitoring presence and concentration of substances in a solution or gas, calculating specific *binding energies*[1], monitoring chemical surface reactions, studying adsorption-desorption processes of substances (isotherms and kinetics). This can in principle be done from the single molecule scale up to the whole cell behavior [5].

Yazdi *et al.* [24] presented a review of a variety of capacitive front-end circuits for high-precision accelerometers. The capacitance readout schemes were compared based on their readout resolution. Also, a high-performance switched-capacitor readout front-end for μg accelerometers with high direct current (dc) stability is described. The circuit was implemented in 0.5 μm, 5 V CMOS process technology and used correlated double sampling (CDS) for amplifier finite gain, $1/f$ noise, offset cancellation, and chopper-stabilization of the switches to improve matching to further reduce the offset. The final result was a hybrid-package interface circuit with a sensitivity of 430 mV/g and a resolution of 1.6 $\mu g/\sqrt{Hz}$ at ambient pressure.

Rufer *et al.* [7] described the design of a silicon membrane thermally actuated at its resonant frequency of 40 kHz. The membrane had a piezoresistive bridge for monitoring deflections. The electronics of the measurement stage was developed in a

[1] *Binding energy* is the mechanical energy required to disassemble a whole into separate parts.

0.8 μm CMOS technology. The voltage output of a Wheatstone bridge was amplified by two differentiators and a differential amplifier. The maximum peak-to-peak voltage at the output of the Wheatstone bridge was about 20 μV. Each differentiator gave a voltage gain of around 12 at the frequency band centered at 40 kHz while the gain of the differential amplifier was 100. The device showed 35 mV/Pa of sensitivity.

Zhang *et al.* [25] designed a *reconfigurable* transducer interface circuit whose supply voltage is 3.3 V. The device was developed with a 3-metal, 2-polysilicon, 0.5 μm CMOS process technology. The digital control circuit, memory, and I/O ports was described in Verilog and the modules were synthesized using the Cadence® Buildgates synthesis tool. Physical design of the analog front-end was carefully considered to maximize performance. For instance, common centroid layout techniques were used to reduce the input offsets and match passive component values. The total chip area was 2.2 $mm \times 2.2$ mm and it dissipated 53 μW in a typical four-sensor application. The interface chip could achieve sensitivities of 30 mV/fF and 18 mV/Ω.

Chiou *et al.* [26] developed a vertical comb drive resonator with piezoresistance sensor. The structure was fabricated through a standard 2-poly, 4-metal, 0.35 μm process and its frequency ranged from 5 kHz to 20 kHz. The first resonance frequency was approximately 14.5 kHz. The resonant frequencies and the corresponding mode shapes were calculated by using a Finite-Element Mode (FEM) simulator. The sensing piezoresistor showed variations in the order of hundreds of ohms, thus a variation of just a few μV was obtained from the sensor. Since the resonator will be used for measuring environmental humidity and virus detection, a need for a signal conditioning circuit to monitor the physical variations was discussed.

Thanachayanont and Sangtong [27] proposed a current-mode Wheatstone bridge for low-voltage current-sensing configuration, named as AZKA cell. This configuration presents several advantages over traditional Wheatstone bridge configurations, such as a simple linearization technique and reduction of resistive sensing elements. Some drawbacks of the AZKA cell were the vital matching of current mirror transistor pairs. The circuit was designed to operate with a single 1.5 V power supply and uses a 0.35 μm process technology. The complete interface circuit proposed was targeted for an implantable pressure sensor with a sensitivity of 5 $\mu V/V/mmHg$.

Narula *et al.* [15] presented the design of a potentiostat interface circuit capable to measure currents generated in reduction and oxidation (redox) reactions. These ionic currents ranged from 1 pA to 200 nA in the electrochemical cell.

Bracke *et al.* [28] illustrated a new generic architecture for an ultra low power capacitance to voltage converter with very low power consumption (less than 100 μW). The design consisted on a fully differential class AB OTA with folded cascode stage and switched capacitor (SC) common mode feedback and a CDS scheme to eliminate the effect of the offset on the sensor interface. The input transistors of the AB OTAs were biased in weak inversion to reduce the power consumption. The total current consumption of this amplifier was 4 μA. Moreover, the paper shows an interesting noise analysis for the AB OTAs and the SC devices.

1.4 Thesis Outline

This thesis work is organized in seven chapters that are described as follows. Chapter 1 presents a descriptive overview of the problem, general and specific objectives, and a literature review of important work performed in this area.

Chapter 2 states the theoretical framework or background of CMOS analog integrated circuit design, focusing on the key concepts required for the understanding of the individual system stages operation. Moreover, the chapter includes the fundamental layout design concepts for analog circuit design.

Chapter 3 gives an overview on mechanical microsensors technology, in order to offer a comprehensive introduction to the basic design of MEMS.

Chapter 4 defines the minimal requirements of the signal conditioning system, and a step-by-step design methodology applied to obtain the electronic schematic circuit diagram of each stage. A modular methodology is implemented on the CMOS circuit design. Once defined all stages of the complete system, they are integrated and the final schematic circuit diagram is obtained.

Chapter 5 introduces the results from the simulation analysis of the individual circuit modules designed and the integrated signal conditioning system, as well as an evaluation and discussion of results.

Chapter 6 introduces the layout concepts applied to the schematic circuit diagram. At the end, the complete theoretical system will developed in layout format.

Chapter 7 contains the conclusions of the thesis and discusses future work.

Chapter 2

Principles of Analog Circuit Design

2.1 Introduction

The design of analog circuits relies on an understanding of the transistor models used. For hand calculations, only first-order models are used to evaluate circuit performance. However, many small details of circuit behavior, such as precise gain, distortion, and noise, depend on second-order transistor characteristics. Therefore, second-order characteristics must be included in the circuit verification. A full model will always be used to verify the circuit performance by means of a circuit simulator, such as Mentor Graphics *ICstudio*®. We cannot learn circuit behavior by just running ICstudio®. The best insight is obtained primarily by performing simple hand calculations. Thus, simple models must be used for qualitative results. ICstudio® can then be used to verify the assumptions made and to validate the circuit performance [22].

This chapter, reviews the principles of analog circuit design. The chapter starts with a description of the fabrication and operation of the MOS transistor. Thenafter, two additional sections defines the basic configurations of CMOS analog circuits. Finally, the last section presents the general techniques applied to design the IC layout.

2.2 The MOS Transistor

Figure 2.1 shows the structure of an n-channel and p-channel MOS transistor using an n-well technology. The p-channel device is formed with two heavily doped p^+ regions diffused into a highly doped n^- material called the *well*. The two p^+ regions are called

drain and source and are separated by a distance L (referred to as device length). At the surface between the drain and source lies a gate electrode that is separated from the silicon by a thin dielectric material (silicon dioxide). Similarly, the n-channel transistor is formed by two heavily doped n^+ regions within a lightly doped p^- substrate. This transistor also has a gate on the surface between the drain and source separated from the silicon by a thin dielectric material (silicon dioxide). Essentially, both transistors are four terminal devices as shown in Figure 2.1. For an *n-well process*, the p-bulk connection is common throughout the integrated circuit and is connected to V_{SS} (the most negative supply). Multiple n-wells can be fabricated on a single circuit, and they can be connected to different voltages, in various ways depending upon the application [2].

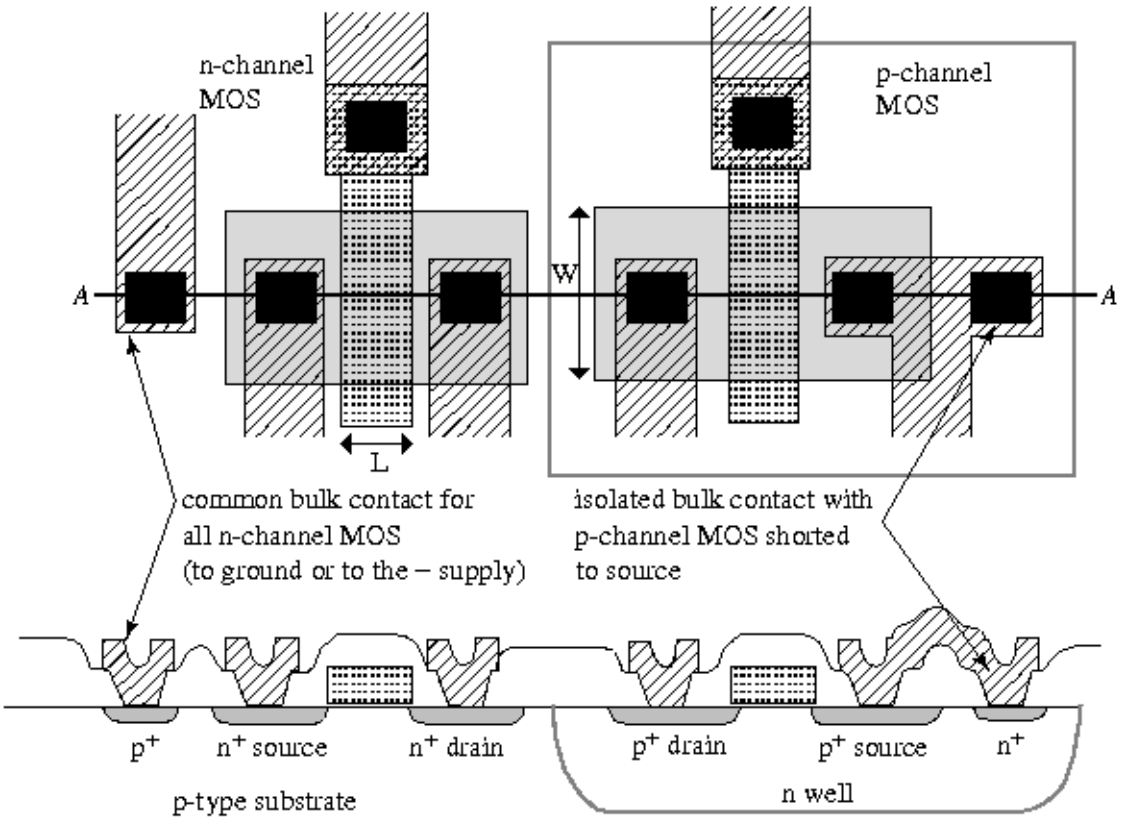

Figure 2.1: Physical structure of MOS transistors.

2.2.1 Operating Regions

The Figure 2.2 shows both, the symbol of an n-channel MOS transistor and the symbol of a p-channel MOS transistor, illustrating their four terminals: *gate*, *source*, *drain* and *bulk*. In the case of the n-channel MOS transistor, when it operates as a switch, the transistor "connects" the source and the drain together if the gate voltage, V_G, is high and isolates the source and the drain if V_G is "low" [1].

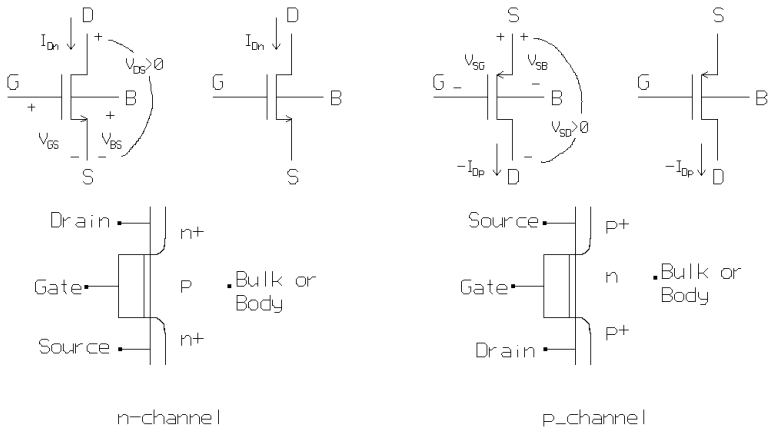

Figure 2.2: The MOS transistor symbol.

Consider a n-channel MOS transistor connected to external voltages. As V_G becomes more positive, the holes in the p-substrate are repelled from the gate area, leaving negative ions behind so as to mirror the charge on the gate. In other words, a *depletion region* is created. Under this condition, no current flows because no charge carriers are available. As V_G increases, so do the width of the depletion region and the potential at the oxide-silicon interface. When the the interface potential reaches a sufficiently positive value, electrons flow from the source to the interface and eventually to the drain. Thus, a *channel* of charge carriers is formed under the gate oxide between source and drain and the transistor is "turned on". At this moment, the interface region is *inverted* [1].

If V_G rises further, the charge in the depletion region remains relatively constant while the channel charge density continues to increase, providing a greater current, I_D, from source to drain. This means that the larger the value of the gate potential, the more the electrons and the "heavier" the inversion is at that point. A few volts of variation of the gate potential can vary the population of electrons there by several

orders of magnitude. Although such variation is continuous, we often say that as the gate potential is raised, transistor goes from *weak* inversion to *moderate* inversion, and eventually to *strong* inversion. This division into three regions is very convenient, because distinct behaviors are observed in each of the three regions [29].

As V_{GS} or V_{DS} is reduced, the current in the channel can eventually become so small that it is masked by the leakage current of the reverse-biased drain-body junction (or even the leakage from the inversion layer to the substrate). In weak inversion region, the current turns out to be due to the diffusion of carriers and I_D is, for all practical purposes, exponentially related to V_{GS}.

In strong inversion, the current turns out to be due to drift. In the *saturation* part of strong inversion, I_D is found to be approximately quadratic in V_{GS} for long-channel devices.

In moderate inversion, both drift and diffusion currents contribute significantly. In this region, I_D is neither exponential nor polynomial; rather its behavior changes gradually from one form of functional dependence to the other, as V_{GS} is raised by a few tenths of a volt. Within this region, the current can vary by a couple of orders of magnitude [29].

2.2.2 Large-Signal Model

As demonstrated in [29], when the length and width of the MOS device is greater than about 10 μm, the substrate doping is low, and when a simple model is desired, the model suggested by Sah [30] is very appropriate. The model equation for an n-channel MOS transistor is developed in Eq. (2.1) as follows

$$I_D = \frac{\mu_0 C_{OX} W}{L}\left[(V_{GS} - V_T) - \frac{V_{DS}}{2}\right]V_{DS} \tag{2.1}$$

Where μ_0 is the surface mobility of the channel, C_{OX} is the capacitance per unit area of the gate oxide, W is the effective channel width and L is the effective channel length. This same model can be used for the p-channel MOS device if all voltages and currents are multiplied by -1 and the absolute value of the p-channel threshold is used.

In order to express the model equations in terms of electrical parameters, there is defined the *transconductance parameter*, K' is defined as follows

$$K' = \mu_0 C_{OX} \tag{2.2}$$

Based on the model of Eq. (2.1) there are three regions of operation for the MOS transistor. These regions depend on the value of $V_{GS} - V_T$. If $V_{GS} - V_T$ is zero or negative, then the MOS device is in the *cut-off*[1] region see Figure 2.3 and Eq. (2.1) becomes

$$I_D = 0, \qquad V_{GS} - V_T \leq 0 \tag{2.3}$$

In this region, the channel acts like an open circuit.

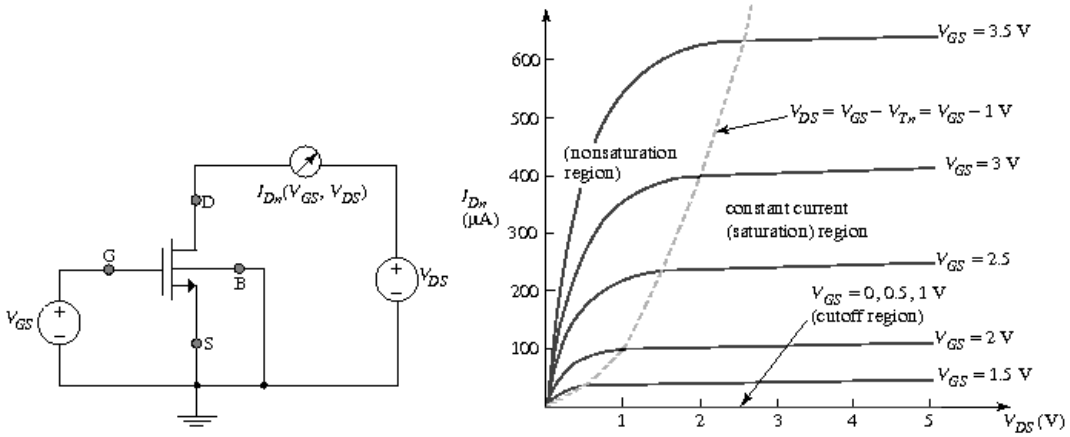

Figure 2.3: Polarization circuit and I_D response of an n-channel MOS transistor.

If V_{DS} is less than $V_{GS} - V_T = V_{DS}(sat)$, then the MOS transistor is in the *nonsaturation* region (see Figure 2.3) and Eq. (2.1) becomes

$$I_D = K' \frac{W}{L} \left[(V_{GS} - V_T) - \frac{V_{DS}}{2} \right] V_{DS}, \qquad 0 < V_{DS} \leq (V_{GS} - V_T) \tag{2.4}$$

The transistor enters in saturation see Figure 2.3 when V_{DS} is greater than $V_{DS}(sat)$ or $V_{GS} - V_T$. At this point the current I_D becomes independent of V_{DS}. Therefore, replacing V_{DS} by $V_{DS}(sat)$ of Eq. (2.1), the result is [2]

$$I_D = K' \frac{W}{2L} (V_{GS} - V_T)^2, \qquad 0 < (V_{GS} - V_T) \leq V_{DS} \tag{2.5}$$

Since the MOS transistor is a bidirectional device, determining which physical node is the drain and which the source may seem arbitrary. However, for an n-channel transistor, the source is always connected to the lower potential of the two nodes, and for the p-channel transistor, the source is always at the higher potential. It is

[1]MOS transistors can operate in the subthreshold region [22, 29].

obvious that the drain and source designations are not constrained to a given node of a transistor, but can switch back and forth depending on the terminal voltages applied to the transistor.

The large-signal model is used to solve for the drain current given the terminal voltages of the MOS device [2]. Equations (2.4) and (2.5) serve as the foundation for analog CMOS design, describing the dependence of I_D upon the constant of the technology, $\mu_n C_{OX}$ [referenced in Eq. (2.2) above], the device dimensions, W and L, and the gate and drain potentials with respect to the source [1].

2.2.3 Linear Characteristics

If in Eq. (2.4), $V_{DS} \ll 2(V_{GS} - V_T)$, we have

$$I_D \approx K' \frac{W}{L}(V_{GS} - V_T)V_{DS} \tag{2.6}$$

That is, the drain current is a *linear* function of V_{DS}. This is also evident from the characteristics of Figure 2.3 for small V_{DS}. As shown in Figure 2.4, each parabola can be approximated by a straight line. The linear relationship implies that the path from the source to the drain can be represented by a linear resistor equal to

$$R_{on} = \frac{1}{K' \frac{W}{L}(V_{GS} - V_T)} \tag{2.7}$$

A MOS transistor can therefore operate as a resistor whose value is controlled by the overdrive voltage [so long as $V_{DS} \ll 2(V_{GS} - V_T)$]. Note that in contrast to bipolar transistors, a MOS device may be on even if it carries no current. With the condition $V_{DS} \ll 2(V_{GS} - V_T)$ we say the device operates in deep triode region [1] or ohmic region [29].

2.2.4 Small-Signal Model

The small-signal model is a linear model that helps to simplify calculations. It is only valid over voltage or current regions where the large-signal voltage and currents can adequately be represented by a straight line. Figure 2.5 shows a linearized small signal model for the MOS transistor.

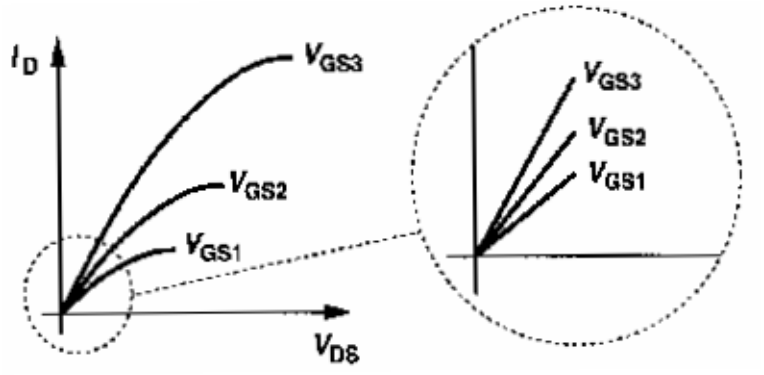

Figure 2.4: Linear operation in deep triode region [1].

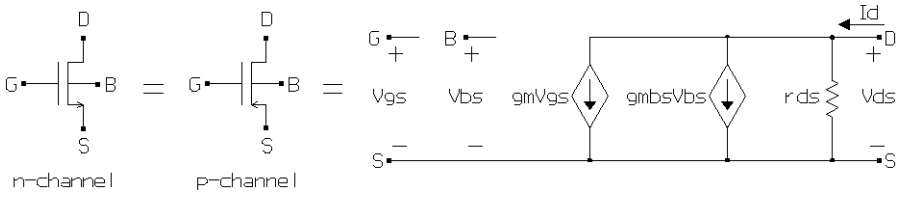

Figure 2.5: Small-signal model of the MOS transistor.

The various parameters of this small-signal model are all related to the large-signal model parameters and dc variables. The channel conductances g_m, g_{mbs} and g_{ds} are defined as (evaluated at the quiescent point) [2]

$$g_m = \frac{\partial i_D}{\partial v_{GS}} \tag{2.8}$$

$$g_{mbs} = \frac{\partial i_D}{\partial v_{BS}} \tag{2.9}$$

$$g_{ds} = \frac{\partial i_D}{\partial v_{DS}} \tag{2.10}$$

The important dependence of the small-signal parameters on the large-signal model parameters and dc voltages and currents is illustrated in Table 2.1, where ϕ_F is the strong inversion surface potential (Fermi potential, measured in V), γ is the bulk threshold parameter ($\gamma_N = 0.4\ V^{1/2}$ for an n-channel device, and $\gamma_N = 0.57\ V^{1/2}$ for a p-channel device), and β is the transconductance parameter (given in terms of physical

Table 2.1: Dependence of the small-signal model parameters operating in the saturation region [2]

Small-signal model parameters	dc current	dc current and voltage	dc voltage
g_m	$\cong (2K'I_D W/L)^{1/2}$	–	$\cong \frac{K'W}{L}(V_{GS}-V_T)$
g_{mbs}	–	$\frac{\gamma(2I_D\beta)^{1/2}}{2(2\lvert\phi_F\rvert+\lvert V_{SB}\rvert)^{1/2}}$	$\frac{\gamma[\beta(V_{GS}-V_T)]^{1/2}}{2(2\lvert\phi_F\rvert+\lvert V_{SB}\rvert)^{1/2}}$
g_{ds}	$\cong \lambda I_D$	–	–

parameters as

$$\beta = K'\frac{W}{L} \qquad (A/V^2) \tag{2.11}$$

The small-signal model for the saturation region will be key element in analyzing circuits in the following chapters.

Moreover, an extremely important assumption for the small signal model parameters is [2]

$$g_m \approx 10\ g_{mbs} \approx 100\ g_{ds} \tag{2.12}$$

Which is very helpful on simplifying numerical calculations.

2.3 Single Stage Amplifiers

Signal amplification is essential in most electronic instrumentation circuits. An analog or digital signal may be too small to drive a load, may require to overcome the noise of a subsequent stage, or may need to match logical levels for a digital input circuit [1]. The inverter is the basic amplifier stage for CMOS circuits. Typically, the inverter uses the common-source configuration with either, an active resistor or a current sink/source [2].

2.3.1 Current-Source Inverter

A current-source inverter amplifier and its voltage transfer curve (VTC) is shown in Figure 2.6. This configuration uses a p-channel MOS transistor as the current-source load. The current source is a common-gate configuration with the gate connected to a dc bias voltage, V_{GG2}. The regions of operation for the transistors of Figure 2.6 are found by expressing the saturation relationship for each transistor. For $M1$, this relationship is

$$V_{DS1} \geq V_{GS1} - V_{TN} \rightarrow V_{OUT} \geq V_{IN} - V_{TN} \tag{2.13}$$

The equivalent relationship for $M2$ requires careful attention to signs. This relationship is

$$V_{SD2} \geq V_{SG2} - |V_{TP}| \rightarrow V_{DD} - V_{OUT} \geq V_{DD} - V_{GG2} - |V_{TP}| \tag{2.14}$$

The maximum output voltage, $V_{OUT}(max)$, of the large-signal output voltage swing for the current-source load inverter is V_{DD} since when $M1$ is off. The voltage across $M2$ can go to zero, allowing the output voltage to be V_{DD}. Thus, the maximum positive output voltage is

$$V_{OUT}(max) \cong V_{DD} \tag{2.15}$$

The lower limit can be found by assuming that $M1$ will be in the nonsaturation region. $V_{OUT}(min)$ can be given as

$$V_{OUT}(min) = (V_{DD} - V_{T1})\left\{1 - \left[1 - \left(\frac{\beta_2}{\beta_1}\right)\left(\frac{V_{SG2} - |V_{T2}|}{V_{DD} - V_{T1}}\right)^2\right]^{1/2}\right\} \tag{2.16}$$

The result assumes that V_{IN} is taken to V_{DD}. The small-signal output resistance of the CMOS inverter with a current-source load can be found as [2]

$$R_{OUT} = \frac{1}{g_{ds1} + g_{ds2}} \cong \frac{1}{I_D(\lambda_1 + \lambda_2)} \tag{2.17}$$

Where λ id defined as the channel length modulation parameter, with typical values (for a channel length of $L = 1\ \mu m$) of $\lambda_N = 0.04\ V^{-1}$ and $\lambda_P = 0.05\ V^{-1}$ for n-channel device and p-channel device, respectively [2].

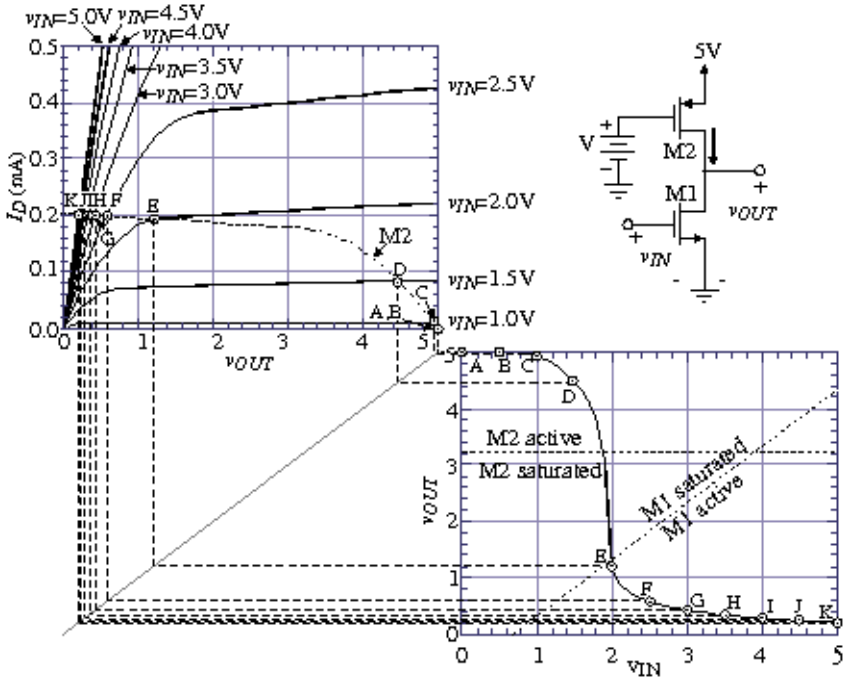

Figure 2.6: Voltage transfer curve and circuit of the current-source inverter [2].

2.3.2 Push-pull Inverter

In comparing the large-signal VTC characteristics between the current-source and the push-pull inverters, a higher gain is obtained by the push-pull inverter assuming identical transistors. This is due to the fact that both transistors are being driven by V_{IN}. Moreover, the push-pull inverter is capable of a rail-to-rail operation and the VTC transition is usually very sharp [2], [31].

The regions of operation for the push-pull inverter are shown on the VTC of Figure 2.7. These regions are easily found using the definition of $V_{DS}(sat)$ given for the MOS transistor. $M1$ is in the saturation region when

$$V_{DS1} \geq V_{GS1} - V_{T1} \rightarrow V_{OUT} \geq V_{IN} - V_{T1} \tag{2.18}$$

$M2$ is in the saturation region when

$$\begin{aligned} V_{SD2} \geq V_{SG2} - |V_{T2}| \rightarrow V_{DD} - V_{OUT} \geq V_{DD} - V_{IN} - |V_{T2}| \\ \rightarrow V_{OUT} \leq V_{IN} + |V_{T2}| \end{aligned} \tag{2.19}$$

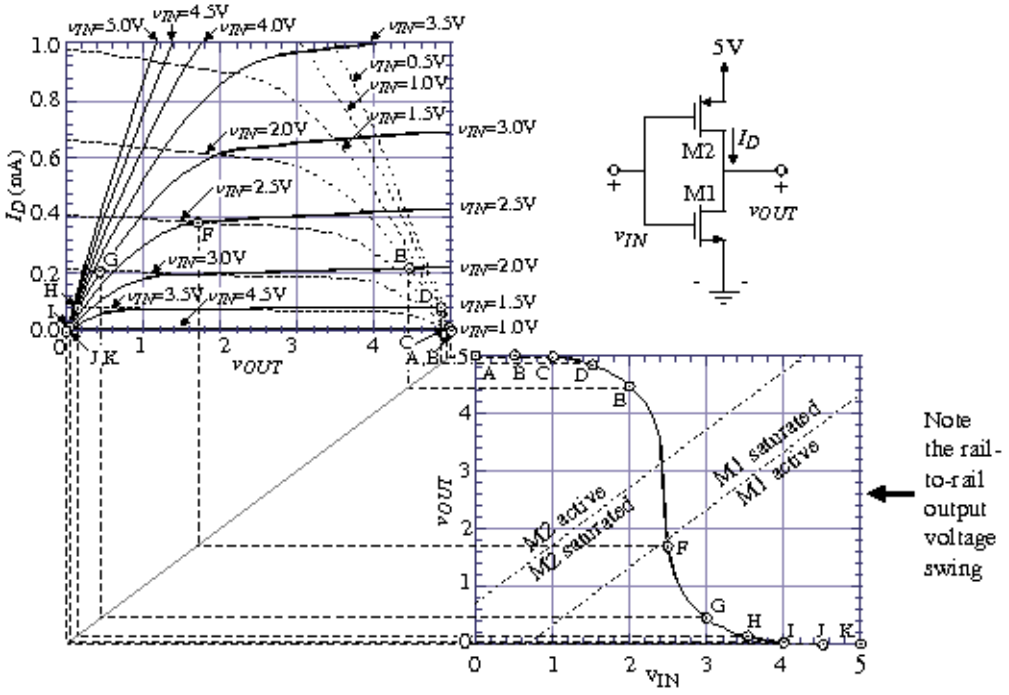

Figure 2.7: Voltage transfer curve and circuit of the push-pull inverter [2].

CMOS Inverter Design Methodology

The inverter threshold voltage, V_{th} is defined as one of the most important parameters that characterize the steady-state input-output behavior of the CMOS inverter circuit. The CMOS inverter can, due to its inherent complementary push-pull operating mode, provide a full output voltage swing between 0 and V_{DD}, and therefore, the noise margins are relatively wide. Thus, the problem of designing a CMOS inverter can be reduced to *setting the inverter threshold*, V_{th}, to a desired voltage value [31]. Given the inverter threshold equation ratio as [31]

$$k_R = \frac{k_n}{k_p} = \left(\frac{V_{DD} + V_{TP} - V_{th}}{V_{th} - V_{TN}} \right)^2 \tag{2.20}$$

Establishing that the switching threshold voltage of an *ideal* inverter is defined as

$$V_{th,ideal} = \frac{1}{2} \cdot V_{DD} \tag{2.21}$$

Since the operations of the n-channel MOS and the p-channel MOS transistors of the CMOS inverter are fully complementary, we can achieve completely symmetric

input-output characteristics by setting the threshold voltages as $V_T = V_{TN} = |V_{TP}|$. The ratio k_R for a symmetrical inverter assumes that the gate oxide thickness, t_{ox}, and hence, the gate oxide capacitance, C_{OX}, have the same value for both n-channel MOS and p-channel MOS transistors. The unity-ratio condition for the ideal symmetric inverter requires that [31]

$$\frac{\left(\frac{W}{L}\right)_n}{\left(\frac{W}{L}\right)_p} = \frac{\mu_n}{\mu_p} \approx \frac{230cm^2/V \cdot s}{580cm^2/V \cdot s} \tag{2.22}$$

Hence,

$$\left(\frac{W}{L}\right)_p \approx 2.5\left(\frac{W}{L}\right)_n \tag{2.23}$$

2.3.3 Differential Amplifier

The differential amplifier is one of the more versatile circuits in analog circuit design. It is also very compatible with IC circuit technology and serves as the input stage to most operational amplifiers (op-amps). Figure 2.8 shows a schematic circuit for a differential amplifier [2].

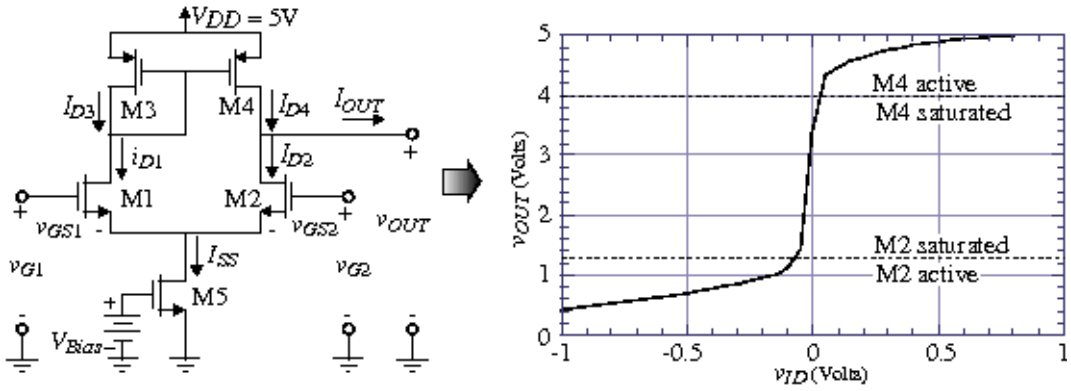

Figure 2.8: Differential amplifier and its voltage-transfer curve [2].

Large-Signal Analysis

If we assume that the currents in the current mirror are identical, then I_{OUT} can be found by subtracting I_{D2} from I_{D1} for the n-channel differential amplifier of

Figure 2.8. Since I_{OUT} is a differential output current, the differential-in, differential-out transconductance is given as

$$g_{md} = \frac{\partial I_{OUT}}{\partial V_{ID}}(V_{ID} = 0) = \left(\frac{K_1' I_{SS} W_1}{L_1}\right)^{1/2} \tag{2.24}$$

Which is exactly equal to the transconductance of the common-source MOS transistor if $I_D = I_{SS}/2$ [2].

The regions of operation for the transistors that conform the differential amplifier are shown on of Figure 2.8. Subscripts applied to the Figure and to the subsequent formulas mean the following: *DS*, for drain to source; *GS*, for gate to source; *S*, for source; *IC*, for input-common mode; *ID*, for input-differential mode; *TN*, for n-channel threshold; *TP*, for p-channel threshold; *OUT*, for the output node.

We note that the largest small-signal gain occurs when both $M2$ and $M4$ are saturated. $M2$ is saturated when

$$\begin{aligned} V_{DS2} \geq V_{GS2} - V_{TN} \rightarrow V_{OUT} - V_{S1} \geq V_{IC} - 0.5V_{ID} - V_{S1} - V_{TN} \\ \rightarrow V_{OUT} \geq V_{IC} - V_{TN} \end{aligned} \tag{2.25}$$

Where we have assumed that the transition region for $M2$ is close to V_{ID}= 0 V.

$M4$ is saturated when

$$\begin{aligned} V_{SD4} \geq V_{SG4} - |V_{TP}| \rightarrow V_{DD} - V_{OUT} \geq V_{SG4} - |V_{TP}| \\ \rightarrow V_{OUT} \leq V_{DD} - V_{SG4} + |V_{TP}| \end{aligned} \tag{2.26}$$

The output swing of the differential amplifier of Figure 2.8 could be given by Eq. (2.25) for $V_{OUT}(min)$ and Eq.(2.26) for $V_{OUT}(max)$. Obviously, the output swing exceeds these values as the magnitude of V_{ID} becomes large [2].

Small-Signal Analysis

The following analysis is only appropriate when both sides of the amplifier are assumed to be perfectly matched. If this condition is satisfied, then the point where the two sources of $M1$ and $M2$ are connected can be considered to be at alternating

current (ac) ground. The unloaded differential voltage gain can be determined by finding the small-signal output resistance of the amplifier. It is easy to see that R_{OUT} is

$$R_{OUT} = \frac{1}{g_{ds2} + g_{ds4}} \tag{2.27}$$

Therefore, the voltage gain is given as the product of g_{md} and R_{OUT}

$$A_V = \frac{V_{OUT}}{V_{IN}} = \frac{g_{md}}{g_{ds2} + g_{ds4}} \tag{2.28}$$

If we assume that all transistors are in saturation and we replace the small-signal parameters of g_m and r_{ds} in terms of their large-signal model equivalents, we achieve

$$A_V = \frac{V_{OUT}}{V_{IN}} = \frac{(K_1' I_{SS} W_1/L_1)^{1/2}}{(\lambda_2 + \lambda_4)(I_{SS}/2)} = \frac{2}{\lambda_2 + \lambda_4}\left(\frac{K_1' W_1}{I_{SS} L_1}\right)^{1/2} \tag{2.29}$$

The dependence of the small-signal gain on the inverse of $I_{SS}^{1/2}$ is similar to the expression found for the inverter. This relationship is in fact valid until I_{SS} approaches subthreshold values.

The common-mode gain of the CMOS differential amplifier of Figure 2.8 is ideally zero. This is because the current-mirror load ideally rejects any common-mode signal. The fact that a common-mode response might exist is due to the mismatches in the differential amplifier. These mismatches consist of a nonunity current gain in the current mirror and *geometrical* mismatches between $M1$ and $M2$ [2].

2.4 Operational Transconductance Amplifier

The *transconductance amplifier*, also called the *operational transconductance amplifier* or *OTA*, shown in Figure 2.9, is a voltage-controlled current source with a specified transconductance gain, g_m. The OTA is essentially a two-stage op-amp with internal compensation. Hence, being somewhat simpler than conventional op-amps, OTAs offer the potential for retaining a very good behavior at frequencies limited by the compensation scheme. Moreover, the design and implementation of bipolar and CMOS OTAs have benefited directly from advances that have occurred in the analog IC area [22].

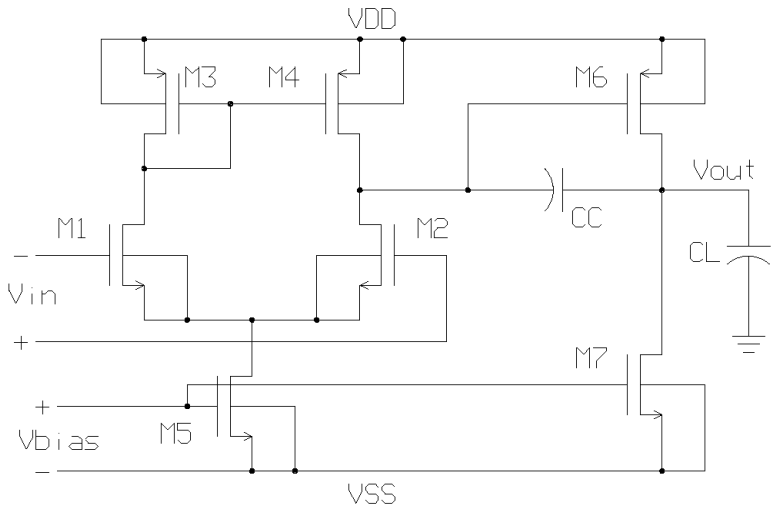

Figure 2.9: Unbuffered, two-stage CMOS OTA with an n-channel input pair [2].

An OTA consists of a two-stage amplifier having a differential input stage, which provides a high gain, connected to a large swing amplifier second stage, that includes a compensation capacitance. This second stage is configured as a simple common-source topology to allow maximum output swing [1]. In analog IC design, using the OTA configuration as an op-amp is a common practice, because it is a simple and robust op-amp implementation, and it can be used as the initial phase for further development of other analog IC devices [2].

2.4.1 The g_m/I_D Design Methodology

This method exploits the transconductance over dc drain current ratio relationship, g_m/I_D, versus the normalized current, $I_D/(W/L)$ [32, 33]. Consider the unbuffered two-stage OTA shown in Figure 2.9. A basic circuit analysis shows that the total dc gain is given by the gain of each individual stage [1, 32]

$$A_I = g_{m1,2}(r_{O1,2}||r_{O3,4}) = g_{m1}R_I = \frac{g_{m1}}{g_{ds2} + g_{ds4}} = \frac{2g_{m1}}{I_5(\lambda_2 + \lambda_4)} \tag{2.30}$$

$$A_{II} = g_{m6}(r_{O6}||r_{O7}) = g_{m6}R_{II} = \frac{g_{m6}}{g_{ds6} + g_{ds7}} = \frac{g_{m6}}{I_6(\lambda_6 + \lambda_7)} \tag{2.31}$$

$$A_V = A_I A_{II} = g_{m1}g_{m6}R_I R_{II} \tag{2.32}$$

By knowing *a priori* the requirements of the OTA as slew rate, unity-gain bandwidth, load capacitance, etc. several design parameters can be defined, as follows [1, 32]

$$SR = \frac{I_5}{C_C} \tag{2.33}$$

$$GB = \frac{g_{m1}}{C_C} \tag{2.34}$$

$$p_2 = \frac{-g_{m6}}{C_L} \tag{2.35}$$

$$z1 = \frac{g_{m6}}{C_C} \tag{2.36}$$

Where $p2$ and $z1$ refer to the output pole, $p2$, and to the right half-plane (RHP) zero, $z1$, of the device [2].

2.5 MOS Device Layout

Analog IC devices have to be designed properly at the physical level in order to function according to the predicted performance provided by simulations. Physical design, in the context of integrated circuits, is referred as *layout* [2]. The layout of a MOS device is determined by both the electrical properties required of the device in the circuit and the *design rules* imposed by the technology [1, 31].

The analog IC technology used to develop a device is characterized by its minimum resolution of a component size. For example, a CMOS 0.35 μm process technology means that the minimum feature size (either *width* or *length*) for a transistor would be 0.35 μm.

2.5.1 MOS Transistor Layout

The Figure 2.10 shows the top view and side view of an n-channel MOS transistor. Moreover, the layout of a p-channel MOS transistor was illustrated in Figure 2.1. The gate polysilicon and the source and drain terminals are tied to metal wires that serve as interconnects with low resistances and capacitances. To accomplish this, one or more *contact windows* must be opened in each region, filled with metal and connected to the

upper metal wires. Note that the gate poly extends beyond the channel area by some amount to ensure reliable definition of the "edge" of the transistor [1].

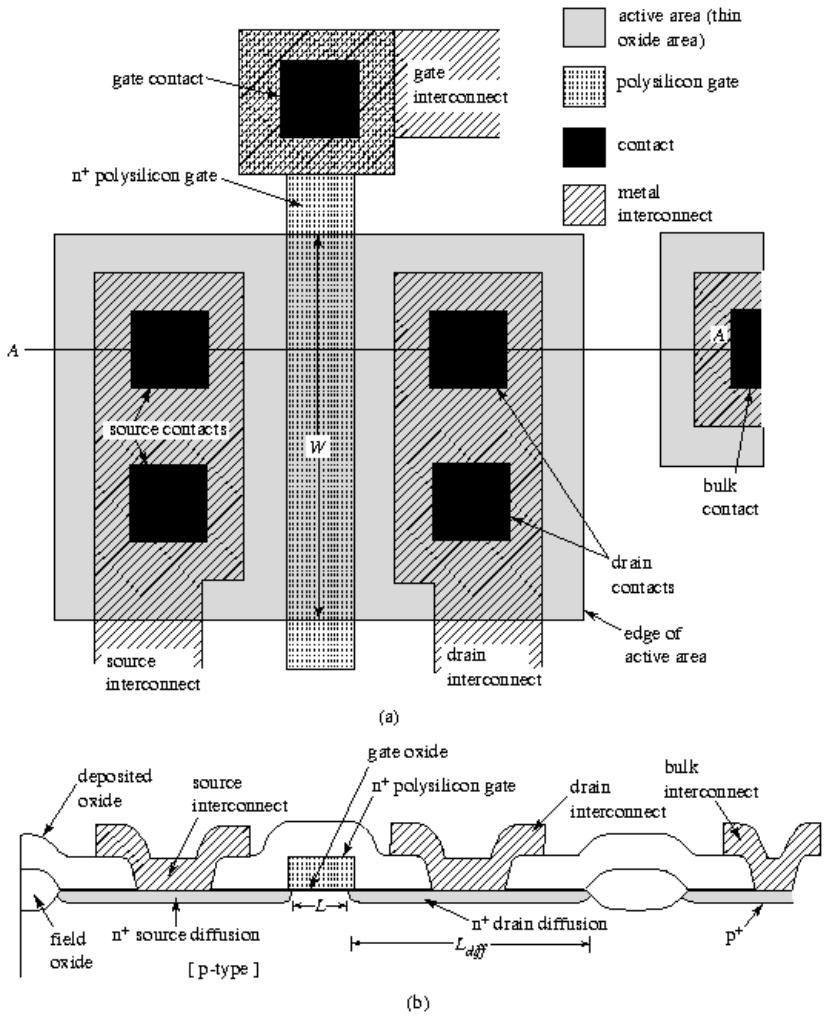

Figure 2.10: Top and side view of an n-channel MOS transistor layout.

2.5.2 MOS Resistor Layout

Figure 2.11 shows the layout of both, a diffusion or polysilicon resistor and a well resistor. To understand the performance of a resistor it is necessary to review the relationship for the resistance of a conductive bar, as shown in Figure 2.12. The resistance, R, measured in ohms (Ω), is given as

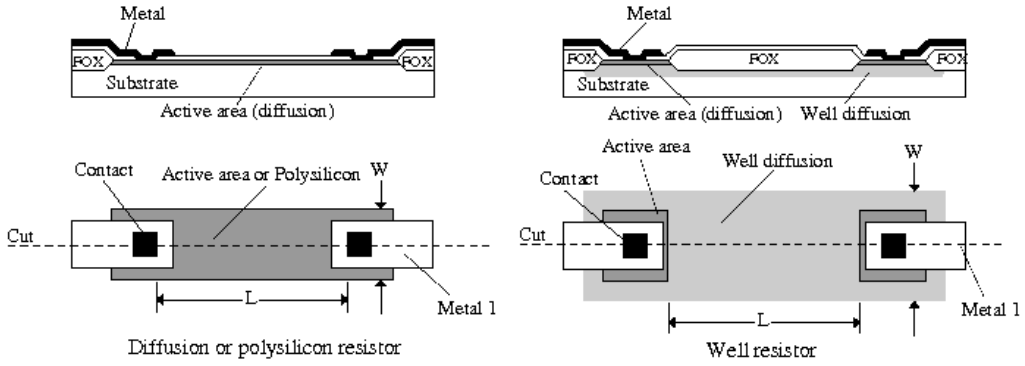

Figure 2.11: Layout of a diffusion resistor and a well resistor [2].

$$R = \frac{\rho L}{A} \tag{2.37}$$

Where ρ is the resistivity in Ω-cm, and A is a plane perpendicular to the direction of current flow. Since the nominal values for ρ and the material thickness, T, are generally fixed for a given process, they are grouped together to form a new term ρ_s called sheet resistivity. This is as follows

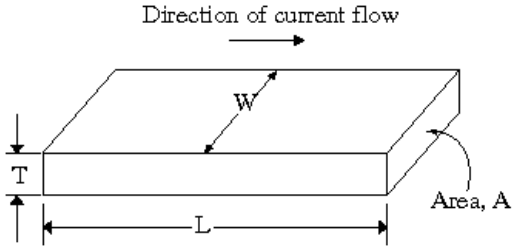

Figure 2.12: Current flow in conductive bar [2].

$$\begin{aligned} R &= \frac{\rho L}{A} = \frac{\rho L}{WT} = \left(\frac{\rho}{T}\right)\frac{L}{W} \\ R &= \rho_s \frac{L}{W} \end{aligned} \tag{2.38}$$

A widely used convention for ρ_s is to use units of $\Omega/\square$ (read *ohms per square*). From the layout point of view, a resistor has the value determined by the number of squares of resistance multiplied by ρ_s [2].

2.5.3 Capacitor Layout

On a double-polysilicon capacitor layout, the second polysilicon layer boundary falls completely within the boundaries of the first polysilicon layer (gate) and the top plate contact is made at the center of the second polysilicon geometry. This is in order to minimize parasitic capacitance.

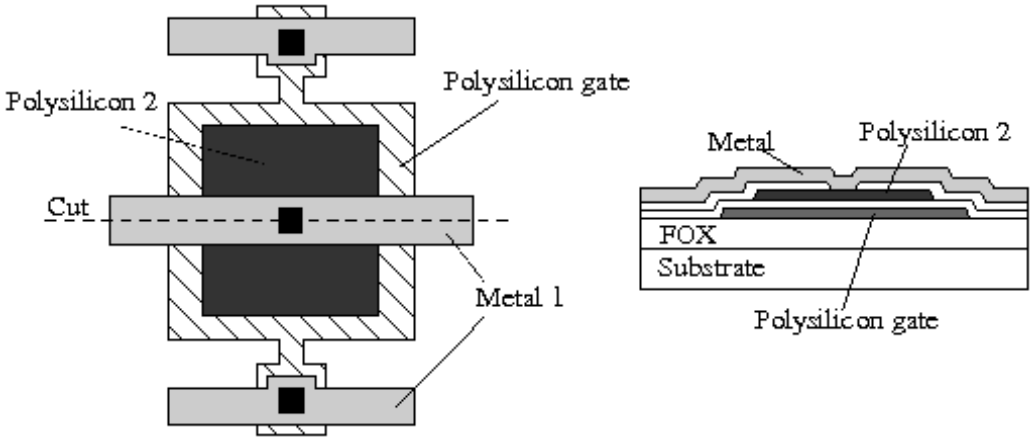

Figure 2.13: Example layout of a double-polysilicon capacitor [2].

The value of IC capacitors is approximately

$$C = \frac{\varepsilon_{OX} A}{t_{OX}} = C_{OX} A \tag{2.39}$$

Where ε_{OX} is the dielectric constant of silicon dioxide (approximately $3.45 \times 10^{-5}\ pF/\mu m$). The performance of analog sampled-data circuits can be directly related to the capacitors used in the implementation [2]. From the standpoint of analog sampled-data applications, one of the most important characteristics of the capacitor is the ratio accuracy [34].

2.5.4 Layout Design Rules

The physical mask layout of any circuit to be manufactured using a particular process must conform to a set of geometric constraints or rules, which are generally called *layout design rules*. These rules usually specify the minimum allowable line widths for physical objects on-chip such as metal and polysilicon interconnects or diffusion

areas, minimum feature dimensions, and minimum allowable clearance between two components [31].

Layout rules governing manufacturability arise, in part, from the fact that at each mask step in the process, features of the next photomask must be aligned to features previously defined on the integrated circuit. Even when using precision automatic alignment tools, there is still some error in alignment. As a result, alignment tolerances impose a limitation of feature size and orientation with respect to other layers on the circuit [2].

2.5.5 General Matching Concepts

Working through the process of designing a circuit, a *circuit designer* must consider all implications that the *physical layout* might have on the circuit operation. Layout and matching are very tightly bound together. A bad piece of layout, from a matching point of view, can ruin a very good design. Conversely, a good layout can immensely enhance a design [23].

The following simple concepts are helpful during layout process. There are also advance matching techniques, which shall be used only when excellent matching is required. These techniques consume a lot of design time and in many occasions they are not required since by applying an easier matching technique, proper circuit performance can be achieved [23].

Floorplaning

The three main problems a *mask designer* has to deal with are: a) photolithographic *unrepeatability* which depends on the IC fabrication process, b) *temperature* of components to match, and c) *noise* generated from nearby devices [23].

Layout improvement opportunities can be achieve by placing matching components together from each other in order to maintain the same temperature on both. Moreover, by keeping the same orientation, the effect observed due to fabrication process variability is reduced [23]. Those matching improvements are observed by comparing the floorplaning shown in Figure 2.14 against the floorplaning shown in Figure 2.15.

Pay attention to devices that are adjacent to the matched components. Even though two matched components might be located next to each other and oriented the

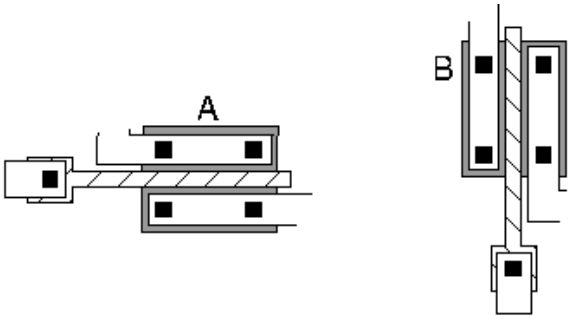

Figure 2.14: Unmatched MOS transistor pair [2].

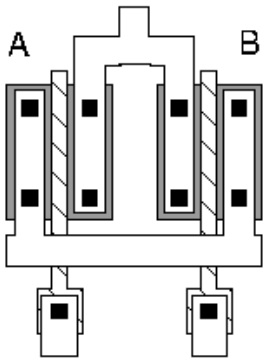

Figure 2.15: Example layout of MOS transistors using mirror symmetry [2].

same, the one on the right, for example, might be closer to a heat source. Consider the Figure 2.16. The two square components have identical shape in area and perimeter as drawn. However, the surroundings seen by A and B are different due to the presence of object C.

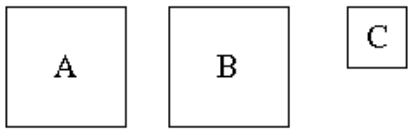

Figure 2.16: Matching of A and B is disturbed by the presence of C [2].

The solution is to force the surroundings of A and B to be the same, this can achieve by adding either equal devices or *dummies* around A and B, as shown in Figure 2.17 [2].

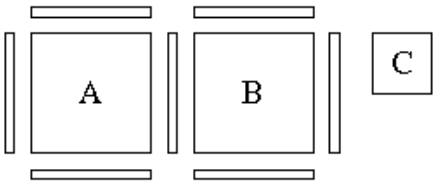

Figure 2.17: Improved matching achieved by matching surroundings of A and B [2].

Those three basic rules guarantee a certain amount of good matching, plus the advantage of better device performance. It is important to clarify that these rules are flexible. If the layout requires to rotate a component or add a neighbor device to a matched components pair, it depends on the circuit designer and the layout designer if this change is not critical to circuit performance [23].

Geometry

When designing a layout, symmetry is very important. Keeping the same length for differential signal paths and choosing a basic root component, known as *unit component*, for making *interdigitation* are proven matching techniques [23]. Consider the matched MOS transistor pair of Figure 2.15. By choosing a unit component equivalent to one fourth of each main component, the MOS transistors of Figure 2.15 can be

split into four smaller components, which can be wrapped or interdigitated in order to increase their matching, as shown in Figure 2.18 [23].

Another important technique is choosing a central point for your circuit in order to achieve better matching [23]. This is called the principle of *common-centroid* layout and is observed in Figure 2.18 at the point located between transistors $B.2$ and $B.3$. The drain and source terminals of components A and B can be combined for making a more compact layout, and the common-centroid is preserved.

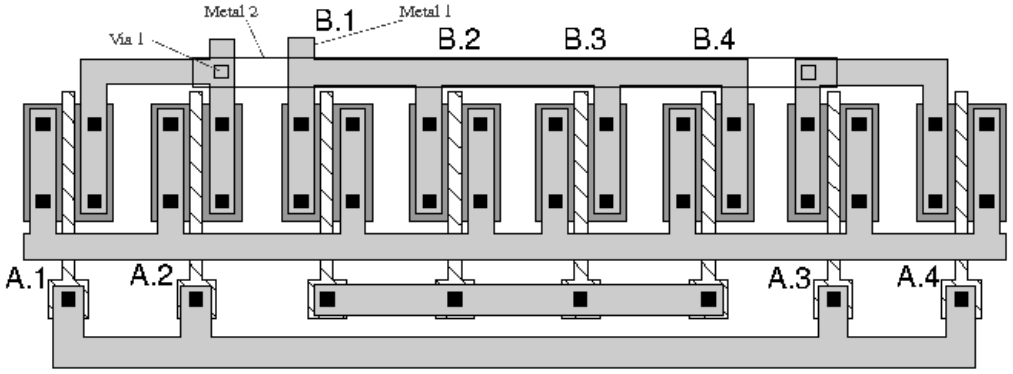

Figure 2.18: Two transistors sharing a common source, split in their unit component and interdigitated [2].

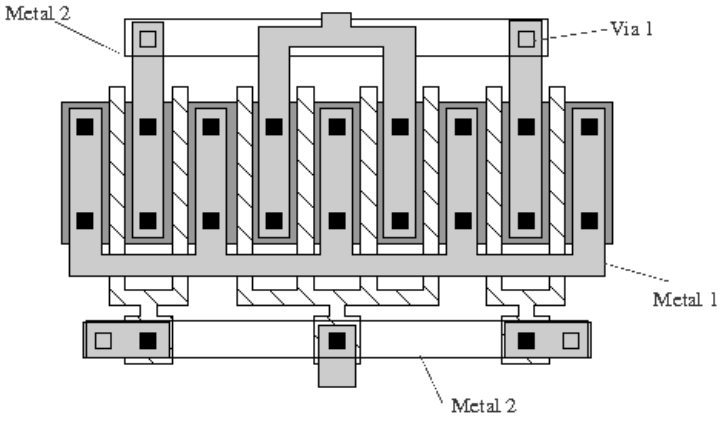

Figure 2.19: Compact layout of Figure 2.18 [2].

The geometrical definition of CMOS devices is learned through practice, and in analog layout design there are a lot of hints and tricks depending on the circuit behavior, process technology and designer experience. New matching techniques emerge from

new process technologies. However, symmetry, common-centroid, and the other basic techniques mentioned will always be applicable on analog layout design [23].

General Matching Rules

The following list contains the fundamental matching rules for layout design. Although those rules are not mandatory, they must be considered for analog circuit design. If any rule is going to be ignored, there must be a well established reason for it, and the consequences should be considered [23].

1. Keep the same structure for all the circuit.
2. Maintain the same temperature in the circuit.
3. Use the same shape, and the same size as well.
4. Use the minimum permissible distance for matched components.
5. Apply common-centroid geometries.
6. Keep the same orientation (photolitographic invariance).
7. Matched components must have same surroundings (dummies are useful).
8. Use the non-minimum size of components.

Chapter 3

Microsystems

3.1 Introduction

This chapter presents an introduction to MEMS technology and an overview to a sensor device which produces the typical signals to be conditioned. The chapter discusses the definition of MEMS, followed by a brief description of the physical properties of silicon, explaining about single crystal silicon and polycristalline silicon. Finally, the piezoresistive sensors are presented to characterize the type of signals that will feed the proposed signal conditioning device.

3.2 Definition of MEMS

A sensor may be simply defined as a device that converts a nonelectrical input quantity into an electrical output signal. Conversely, an actuator may be defined as a device that converts an electrical signal into a nonelectrical quantity. A transducer is a device that can be a sensor, an actuator, or both [4].

The term *Microelectromechanical Systems* (MEMS), refers to the integration of mechanical elements, sensors, actuators, and electronics on a common silicon substrate through microfabrication technology. While electronic circuits are fabricated using IC processes (e.g., CMOS, Bipolar, or BiCMOS processes), the micromechanical components are fabricated using compatible "micromachining" processes that selectively etch away parts of the silicon wafer or add new structural layers to form the mechanical and electromechanical devices [35].

3.3 Physics of Silicon

Materials occur in either a crystalline or an amorphous state. The crystalline state refers to the organization of $\sim 10^{22}$ $atoms/cm^3$ arranged in a regular manner in a three-dimensional structure. If the periodic arrangement occurs throughout the volume of a sample material, this constitutes a *single crystal*. If the regular structure occurs only in portions of a material and the different portions are aligned arbitrary with respect to each other, the material is said to be *polycrystalline*. The individual regular portions are referred to crystallites or "grains" and are separated from each other by grain boundaries.

If the individual crystallites are reduced in size to the point where they approach the size of a unit cell (an elementary block, which contains atoms placed at fixed positions), periodicity disappears and the material is called amorphous or glassy [4].

3.3.1 Single Crystal Silicon

For MEMS applications, single crystal silicon has several key functions. Single crystal silicon is perhaps the most versatile material for bulk micromachining, due to the possibility of making well-characterized anisotropic etches and to be available as etch-mask materials. In surface micromachining applications, single crystal silicon substrates are used as mechanical platforms on which device structures are fabricated, whether they are made from silicon or other materials [36].

Also, in etching process, the directionality (or profile) is an important characteristic: the etching process can be isotropic or anisotropic. In terms of anisotropic etching, the angles in the profile between {100} and {110} planes are 45° or 90°; the angles between {100} and {111} planes are 54.7° or 125.3°; planes {111} and {110} can intersect each other at 35.3°, 90° or 144.7°. The angle between {100} and {111} is important because many alkaline aqueous solutions (such as KOH), selectively etch the {100} planes of silicon but not the {111} planes. The etch results in cavities that are bounded by {111} planes [37].

3.3.2 Polycrystalline Silicon

Also named polysilicon, is made up of small single crystal domains, or grains, whose orientations and/or alignment vary with respect to each other. The roughness

often observed on polysilicon surfaces is due to the granular nature of polysilicon [36]. At the grain boundaries, the grains of different orientations meet resulting in an extremely thin amorphous layer. These boundaries create electrical barriers and therefore have a significant influence on the mechanical properties. The basic structure can be small random grains or columns (see figure 3.1).

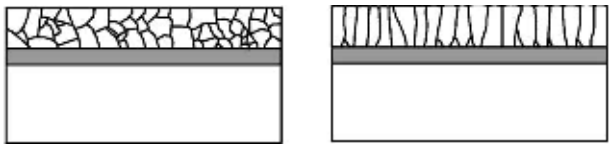

Figure 3.1: Two polysilicon structures [3].

The microstructure of the deposited polysilicon is a function of the deposition conditions, such as the pressure, flow and temperature. Polysilicon can be deposited using chemical vapor deposition, being the low pressure systems (LPCVD) preferred for microfabrication purposes.

Polysilicon has been shown to be a highly flexible material for microsystem applications. From the early days, as interconnect, gates and capacitors, it has expanded to mechanical sensors and actuators with the help of micromachining techniques. The piezoresistive effect in polysilicon is lower than that of single crystal silicon. However, it has the advantage of not requiring a p-n junction as isolation and has greater flexibility since there is no single crystal orientation. In micromachining, polysilicon has been found highly suitable as a mechanical and sacrificial layer, although the role as a mechanical material has received more attention. Since the 1980s, polysilicon has been widely used for micromechanical structure in both, sensor and actuator applications [3].

The resistivity of polysilicon can be modified by impurity doping using the methods developed for single crystal doping. The addition of dopants during the deposition process affects the conductivity of the deposited films, and the deposition rate. Relative to the deposition of undoped polysilicon, the addition of phosphorous (P) reduces the deposition rate, while the addition of boron (B) increases the deposition rate [3, 38].

3.3.3 Electrical properties

Polysilicon can be modelled as a series of resistors, as shown in Figure 3.2.

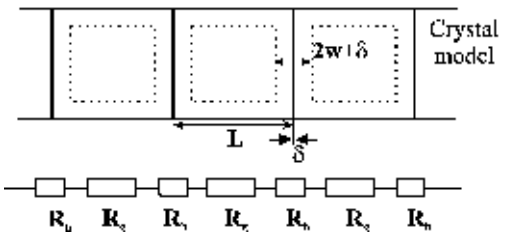

Figure 3.2: Simple electrical model for polysilicon [3].

Resistivity is also strongly affected by the grain boundary. The grain boundary can be considered as a Schottky barrier with a semiconductor on both sides as shown in Figure 3.3.

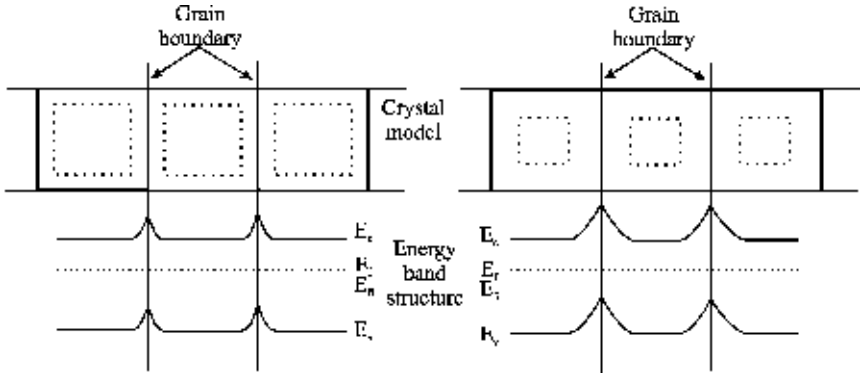

Figure 3.3: Model structure showing the band bending due to the barrier [3].

In normal operation, the voltage drop across each grain boundary is small. The boundary can be treated as a linear resistor, and thus in a simplified form, assuming a linear resistor, the resistivity, ρ, of a polysilicon film can therefore be defined by

$$\rho = \left[\frac{L-(2w+\delta)}{L}\right]\rho_g + \left[\frac{2w+\delta}{L}\right]\rho_b \tag{3.1}$$

Where L, w and δ are as defined in figure 3.2, and ρ_g and ρ_b are the grain and barrier resistivity, respectively [3].

3.3.4 Mechanical properties

Young's modulus of silicon is highly dependent upon crystal orientation. The value for polysilicon has been found to fall between the maximum and minimum theoretical

crystalline values, which indicates that the grain boundary does not have a significant effect.

The intrinsic stress, on the other hand, has been found to be highly dependent upon how the grain boundaries are formed. High stress levels in films on the surface of the silicon wafer can cause significant problems in devices below. For micromachining it is also extremely important, even when at relatively low levels. When polysilicon is in compressive stress, double clamped structures will tend to buckle. Only structures under a critical length will remain flat. The ideal behavior for most applications is low tensile stress. This will ensure that the mechanical structures are pulled into the correct shape, although high tensile stress will lead to breakage [39].

3.3.5 Piezoresistivity

The property where a fractional change in bulk resistivity is induced by small mechanical stresses applied refers to piezoresistivity of the material. The piezoresistive effect in semiconductor materials originates the deformation of the energy bands as a result of the applied stress. The deformed bands change the effective mass and mobility of the charge carriers (electrons and holes), hence modifying the resistivity [36].

In anisotropic materials, resistivity ρ_i is defined by a tensor that relates the three components of electric field, ε_i, with the three components of current flow, j_i; this is called the *resistivity matrix* [40]. When stress is applied to silicon, the components in the resistivity matrix change. The change in each of the independent components $\Delta\rho_i$, will be related to all the stress components. A preferred representation is to express the fractional change in an arbitrarily oriented diffused resistor by

$$\frac{\Delta R}{R} = \pi_l \sigma_l + \pi_t \sigma_t \tag{3.2}$$

Here, π_l, denotes longitudinal piezoresistance coefficient; σ_l is the stress component parallel to current flow (in longitudinal direction). And π_t, σ_t, are the values in the transversal direction [38].

Neglecting the transverse stress, the change in resistance due to piezoresistance, only depends upon the longitudinal term as follows [39]

$$\frac{\Delta R}{R} = \pi_l \sigma_l \tag{3.3}$$

This is a useful approximation when the piezoresistive material is made of polycrystalline silicon.

The piezoresistive coefficient of polysilicon grain is estimated by taking the average value for each grain. In some polysilicon structures there is a texture, which means that a small number crystal orientations, whereas other films have been found to have a totally random structure.

3.4 Piezoresistive Sensors

The working principle of piezoresistive sensors relies on the mechanical deformation of their construction (deflection of a membrane or a mass suspended by a beam). This deformation is translated to a resistivity change, and thenafter, to an electrical signal [41].

The use of strain gauges in conventional sensors is a very common practice. The resistance of a conductor depends on its geometry, so conductors assembled in deforming bodies will give information about the deformation. Semiconductors have an additional material effect: the conductivity depends on the strain in the material. This effect is called *piezoresistivity*. The relative change of the resistance per strain is called the *gauge factor*. For conventional metal strain gauges, the gauge factor is of the order of one, while the piezoresistive effect in silicon increases the gauge factor of silicon strain gauges to one hundred. The disadvantage of the piezoresistive effect is its temperature dependence.

Piezoresistive sensors benefit from simple design, straight-forward electronic signal processing, and ease of integration. Piezoresistors are generally placed at locations that are under the most stress during sensor operation and are electrically isolated from the main body, which generally is a membrane, a bridge, or a similar structure, as shown in Figure 3.4. Electrical isolation is achieved by either depositing the piezoresistors on top of a layer of insulating material or using reverse biased junctions [39].

3.4.1 Wheatstone Bridge Configuration

Resistance changes are often read using the Wheatstone bridge circuit configuration. Polysilicon piezoresistances are temperature dependent, and a well-known technique to compensate for temperature variations is to use a Wheatstone bridge con-

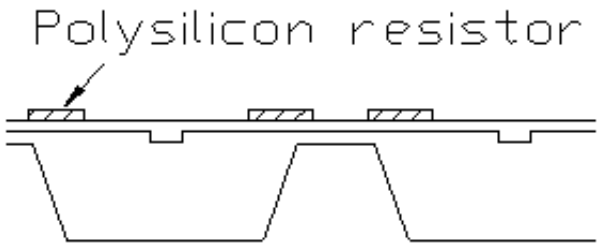

Figure 3.4: Simple representation of a piezoresistive sensor membrane.

figuration [27]. Since the bridge output voltage is proportional to the relative change in resistance, and the change in resistance is generally in the order of 0.01 % to 0.1 %, the bridge output voltage is quite small and needs to be amplified. Therefore, an instrumentation amplifier follows the Wheatstone bridge circuit [42].

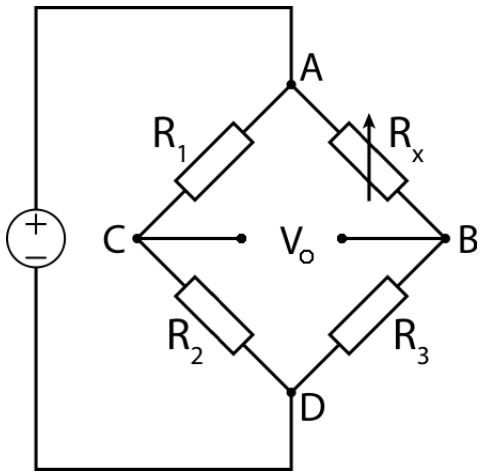

Figure 3.5: Wheatstone bridge circuit configuration.

3.4.2 Operation Modes of Piezoresistive Sensors

When a piezoresistive material like doped silicon is strained, it changes its electrical conductivity. Piezoresistive sensors are therefore ideally suited to monitor stresses, and as mentioned before, their resistivity can be easily measured with a simple Wheatstone bridge [5]. The three basic structures used to design piezoresistive sensors are: the *cantilever beam*, the *bridge*, and the *diaphragm* or membrane. For piezoresistive microcantilevers, two fundamental operation modes domain

a) The *static* mode

a) The *dynamic* mode

On the static operation mode, the free end of the cantilever beam will deflect by a distance Δx when a point load F_x is applied to it (see Figure 3.6). Ignoring gravitational forces and assuming that there is no residual stress in the beam, then the deflection is simply given by [4]

$$\Delta x = \frac{l^3}{3E_m I_m} F_x \tag{3.4}$$

Where E_m is the Young's modulus of the material and I_m is the second moment of area of the beam and related to its width, w, and thickness, d, by

$$I_m = \frac{wd^3}{12} \tag{3.5}$$

The simple cantilever beam can thus be used to convert a mechanical force into a displacement [4].

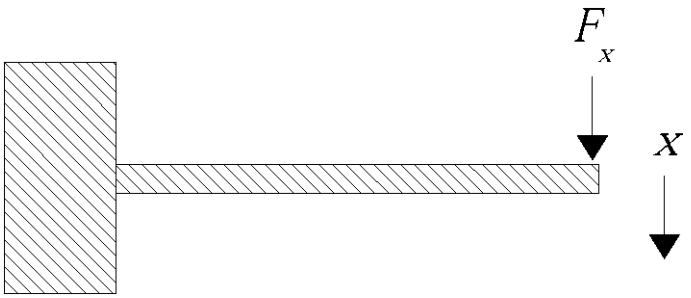

Figure 3.6: Deflection of a cantilever beam by a vertical point force, F_x [4].

On the dynamic operation mode, vibrations at frequency f shaking a mechanical system are damped by a factor which is proportional to f_0/f, where f_0 is the system fundamental resonance frequency. Resonant frequency should therefore be as high as possible. For rectangular cantilevers, f_0 is given by [5]

$$f_0 \approx 0.16 \times \sqrt{\frac{E}{\rho}} \frac{t}{L^2} \tag{3.6}$$

Where ρ is the density of the cantilever material.

High sensitivity and at the same time low noise can be achieved by using small cantilevers. Small cantilevers have also the advantage to respond faster, due to the high resonance frequencies. Microfabricated silicon cantilevers as those shown in Figure 3.7 have resonance frequency in the 30 $kHz - 140$ kHz range in air [4].

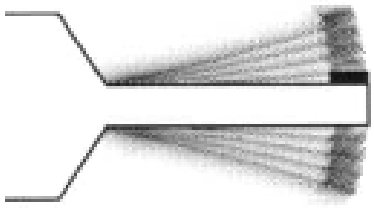

Figure 3.7: Schematic of a resonant mass sensor microcantilever [5].

Applications of Piezoresistive Sensors

Biosensors have attracted considerable interest in the last few years since the monitoring of a specific substance is central in many applications ranging from clinical analysis to environmental control and for monitoring many industrial processes [5].

Reference [6] discusses a technique for the readout of the nanomechanical response of multiple microcantilevers. This combines the optical beam deflection technique and the scanning of a laser beam illuminating the cantilevers of an array sequentially. The technique provides sub-angstrom resolution in the cantilever deflection and it allows the readout of tens of cantilevers per second. This is applied for the quasi-simultaneous detection of single-stranded DNA with an array of five microcantilevers.

Moreover, this technique also allows the measurement of the resonant frequency of individual microcantilevers into an array (in the range of 9 kHz). This can be applied for multiple detection of several pathogen targets. The designed structures had a length of 400 μm, a width of 100 μm and a thickness of about 1 μm. The frequency response and readout diagram are shown in Figure 3.8.

Over the years, piezoresistive sensing has been used for many categories of sensor applications [41]. This technique was applied in [7] for sensing the vibrations in a membrane of an ultrasonic transducer. For vibrations reception, a piezoresistive bridge placed on the membrane is used for monitoring its deflections.

A behavioral model was realized considering three different types of energy coupling: electrothermal, thermomechanical, and piezoresistive. The piezoresistive cou-

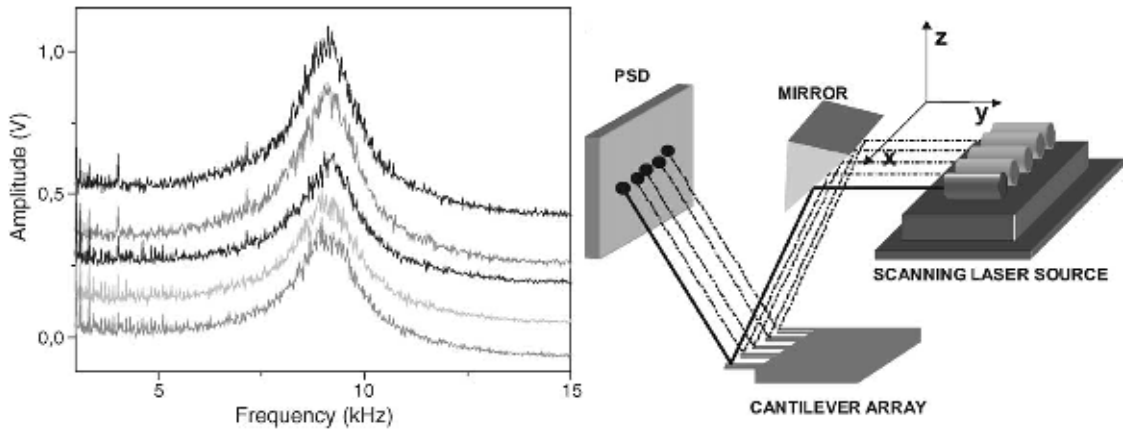

Figure 3.8: Frequency response and system for the sequential readout of microcantilever arrays [6].

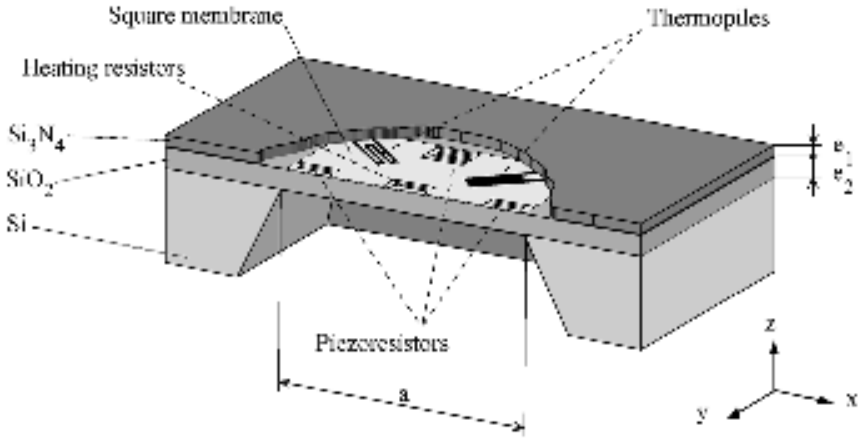

Figure 3.9: Components of a MEMS membrane [7].

pling used a Wheatstone bridge formed by four resistors placed respectively on the center of the four clamped edges (see Figure 3.9). Two resistors were parallel to the membrane edge (longitudinal gauges). The other two piezoresistors were placed perpendicularly to the membrane edge (transversal gauges).

To determine the piezoresistive coupling coefficient for each piezoresistor, a FEM mechanical analysis was required to obtain the stress distribution on the membrane. Based on the stress distribution in the x-direction and y-direction, the relative change of resistance for each piezoresistor is given by

$$\frac{\Delta R}{R} = \frac{1}{N}\sum_{i=1}^{N}(\sigma_{li}\pi_l + \sigma_{ti}\pi_t) \tag{3.7}$$

N is the number of finite elements forming the piezoresistor σ_{li} and σti are the stresses on ith element in the longitudinal and transversal direction, respectively. The constants π_l and pi_t are the piezoresistive longitudinal and transversal coefficients, respectively.

Rufer *et al.* showed simulations where the maximum peak-to-peak voltage at the output of the Wheatstone bridge was about $V_O = 20\ \mu V_{PP}$. The bridge was powered with 5 V dc and the gain of the amplification chain at 40 kHz was about 83 dB [7]. Figure 3.10 shows the response of the membrane to an external vibration source illustrating its resonant frequency approximately at 42 kHz.

Those obtained results show the feasibility of an integrated MEMS-based system using thermoelectrical excitation and piezoresistive sensing at 40 kHz. This frequency is high enough to avoid potential interferences with industrial noise. The device was fabricated in an integrated form using a 0.8 μm CMOS technology by using only the dielectric layers of a CMOS process to build a membrane structure. Due to the use of an amplifier placed at the output of the piezoresistive Wheatstone bridge, the device shows a sensitivity in the sensor mode of 35 mV/Pa [7].

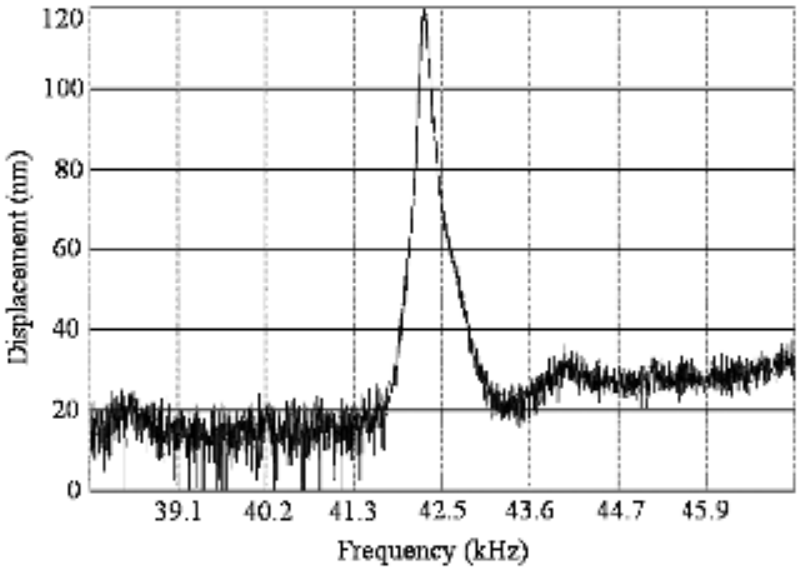

Figure 3.10: Displacement of the membrane shown in Figure 3.9 [7].

Chapter 4

Signal Conditioning Circuit Design

4.1 Introduction

This chapter describes the design of the electronic interface circuit required to measure a frequency signal from a resonant output sensor. The chapter discusses the operational transconductance amplifier design, and the instrumentation amplifier configuration which will be connected to the sensor terminals. The chapter also illustrates the design of additional inverter circuit stages used to convert the low amplitude output signal from the instrumentation amplifier to a squarewave signal. This is to obtain a "clean" frequency signal with an amplitude of $\pm 1.5\ V$. Finally, the last section explains the integration of the complete electronic circuit, which conforms the signal conditioning device. The electronic circuit is designed using the Design Architect [43] tool, from ICstudio®, and the CMOS AMS® 0.35 μm technology process parameters [44]. A block diagram of the complete system is shown in Figure 4.1.

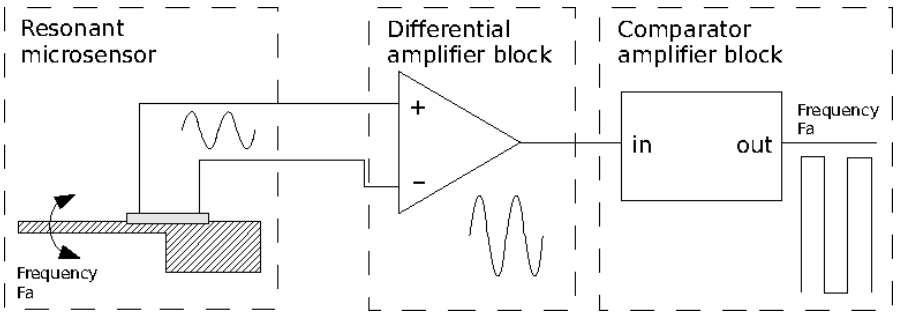

Figure 4.1: Block diagram of the complete proposed system.

On the Figure, the input signal comes from a resonant microsensor and amplified with a differential input amplifier, then, the ground referenced signal is amplified again by a comparator block circuit, and a squarewave frequency signal is obtained on the circuit output terminal.

4.2 Operational Transconductance Amplifier

In order to design an OTA that complies with noise requirements, a p-channel input is selected and the g_m/I_D design methodology is used as well. This section discusses the general requirements for the amplifier. Next, the design of an p-channel input differential pair and a current-source load stage is presented to obtain the OTA circuit. Other circuit blocks are designed: the bias voltage source used to operate transistors in the nonsaturation region (as resistors), and the bias current sink to provide power bias for the OTA circuit.

4.2.1 General Requirements

As mentioned in Chapter 3 and according to [15, 7, 24, 25], a typical resonant sensor signal can have 10 μV of voltage amplitude or 8 pA of current amplitude. Moreover, its frequency could be as low as 40 kHz, depending on the sensing mechanism. The Table 4.1 presents the main OTA design specifications. These parameters are useful as a starting point, but they have some sort of flexibility according to the trade-offs encountered during the design procedure. Since design techniques are applied to improve a few requirements, the final design meets the specifications shown in Table 4.1.

Moreover, for obtaining a numerical approximation, additional CMOS fabrication process specifications are assumed. Those are shown in Table 4.2.

The initial assumption is that all MOS transistors are perfectly matched. Therefore

$$g_{m1} = g_{m2} = g_{mI} \tag{4.1}$$

$$g_{m6} = g_{mII} \tag{4.2}$$

$$g_{ds2} + g_{ds4} = G_I \tag{4.3}$$

$$g_{ds6} + g_{ds7} = G_{II} \tag{4.4}$$

Table 4.1: OTA design specifications

Specification	Abbreviation	Value
Minimum dc gain	$A_V(0)$	2500 V/V
Unity gain bandwidth	GB	2 MHz
Phase margin	Φ_M	60°
Input common-mode voltage range	$ICMR$	± 0.3 V
Load capacitance	CL	10 pF
Slew rate	SR	5 $V/\mu s$
Output voltage swing	V_{OUT}	$\pm 0.8V$
Positive supply voltage	V_{DD}	1.5 V
Negative supply voltage	V_{SS}	-1.5 V
Power dissipation	P_{diss}	2 mW
Device length	L	1 μm

Table 4.2: CMOS process parameters [2]

Parameter	Abbreviation	Value
p-type transconductance parameter	K'_p	50 $\mu A/V^2$
n-type transconductance parameter	K'_n	110 $\mu A/V^2$
Gate oxide thickness	t_{ox}	140$\mathring{A}$
n-type threshold voltage	V_{TN}	0.7 V
p-type threshold voltage	V_{TP}	-0.7 V
n-channel length modulation parameter	λ_P	0.04 V^{-1}
p-channel length modulation parameter	λ_N	0.05 V^{-1}

The matching relationships are based on the circuit shown in Figure 4.2. Since analog design is an iterative process, a slight change in circuit parameters could strongly affect the circuit behavior. Numerical calculations as well as simulations are very useful to help designers achieving the required performance, and to verify designs in a reasonable period of time.

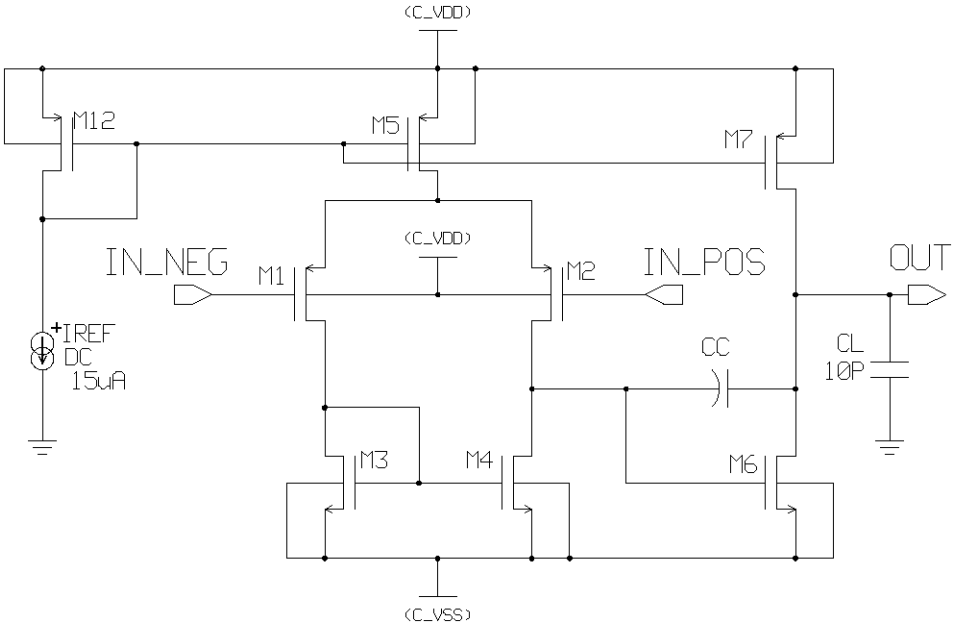

Figure 4.2: Unbuffered, two-stage CMOS OTA with a p-channel input pair.

4.2.2 Differential Pair Stage

Once determined all the OTA requirements, the following step is to establish the minimum value for the compensation capacitance, CC. Reference [32] shows that placing the output pole p_2, 2.2 times higher than the GB, achieves a 60° phase margin. This pole placement results in the minimum requirement for CC. Therefore, by taking the load value from Table 4.1, the minimum compensation capacitance is evaluated as follows

$$\begin{aligned} CC &> (2.2/10) \times CL \\ CC &> (2.2/10) \times 10\ pF \\ CC &> 2.2\ pF \end{aligned} \tag{4.5}$$

Now, the slew rate specification provides a useful minimum value for the current I_5

$$\begin{aligned} I_5 &= SR(CC) \\ I_5 &= (5\ V/\mu s)(2.2\ pF) \\ I_5 &= 11\ \mu A \end{aligned} \tag{4.6}$$

The aspect ratio of $M3$ can be determined by using the requirement for input common-mode range as follows

$$I_3 = \frac{I_5}{2} \tag{4.7}$$

Thus, from Eq. (2.5) we obtain

$$S_3 = (W/L)_3 = \frac{2I_3}{K_3'}\left[-V_{SS} + V_{IN}(min) - V_{T3}(max) + |V_{T1}(min)|\right]^2 \tag{4.8}$$

$$S_3 = (W/L)_3 = \frac{11\ \mu A}{(110\ \mu A/V^2)\left[-(-1.5\ V) + (-0.3\ V) - 0.85\ V + |-0.55\ V|\right]^2}$$

$$S_3 \approx 0.1235$$

This value does not comply with $S_3 \geq 1$, therefore, a change for $S_3 \geq 1$ will be considered for future iterations.

Since all transistors are perfectly matched, device $M4$ has the same transconductance and aspect ratio as device $M3$. Thus

$$S_4 = S_3 \tag{4.9}$$

At this point, it is important to verify that the pole and zero due to C_{gs3} and C_{gs4} will not be dominant [2]. This verification is done by comparing p_3 against the gain bandwidth, GB. First determine transconductance and capacitance of $M3$, from Table 2.1 and the definition of gate-oxide capacitance, which is

$$C_{OX} = \frac{\varepsilon_{OX}}{t_{OX}} = \frac{3.9\varepsilon_O}{t_{OX}} \tag{4.10}$$

The value for g_{m3} is

$$\begin{aligned} g_{m3} &= \sqrt{2(110\ \mu A/V^2)(5.5\ \mu A)(0.1235)} \\ g_{m3} &\approx 12.222\ \mu S \end{aligned} \tag{4.11}$$

The value of C_{gs3}, obtained by Eq. (4.10), is

$$\begin{aligned} C_{gs3} &= \left(\frac{2}{3}\right) W_3 L_3 C_{OX} = \left(\frac{2}{3}\right) W_3 L_3 \left(\frac{3.9\varepsilon_O}{t_{OX}}\right) \\ C_{gs3} &= \left(\frac{2}{3}\right)(0.1235\ \mu m)(1\ \mu m)\frac{(3.9)(8.854\ pF/m)}{140\ \mathring{A}} \\ C_{gs3} &\approx 2.03 \times 10^{-16}\ F = 203\ aF \end{aligned} \tag{4.12}$$

Then, pole p_3 is

$$p_3 \approx \frac{g_{m3}}{2C_{gs3}} = 3.0104 \times 10^{10}\ rad/sec \tag{4.13}$$

converting from rad/sec to Hz we have

$$p_3 = \frac{3.0104 \times 10^{10}\ rad/sec}{2\pi} = 4.7912\ GHz \tag{4.14}$$

And, comparing against the specification of GB

$$\begin{aligned} p_3 &>> 10GB \\ 4.7912\ GHz &>> 20\ MHz \end{aligned} \tag{4.15}$$

This verifies that pole $p3$ is greater than GB by a factor of ten. The following components to be considered are $M1$ and $M2$. The transconductance of $M1$ is given by

$$g_{m1} = GB \cdot CC \tag{4.16}$$

And aspect ratios for $M1$ and $M2$ are

$$S_1 = S_2 = \frac{g_{m1}^2}{K_1' I_5} \tag{4.17}$$

From Eqs. (4.16) and (4.17), the values of g_{m1} and S_1 are

$$\begin{aligned} g_{m1} &= (2\ MHz)(2\pi)(2.2\ pF) \\ g_{m1} &= 27.646\ \mu S \end{aligned}$$

$$S_1 = \frac{(27.646\ \mu S)^2}{(50\ \mu A/V^2)(11\ \mu A)} \approx 1.3896$$

$$S_1 = S_2 \approx 1.3896 \tag{4.18}$$

The last component from the differential pair is the current source, $M5$, and the aspect ratio can be derived from its maximum saturation voltage as follows

$$V_{DS5}(sat) = V_{DD} - V_{IN}(max) - \sqrt{\frac{I_5}{K_1' S_1}} - |V_{T1}(max)| \tag{4.19}$$

$$\begin{aligned} V_{DS5}(sat) &= 1.5\ V - 0.3\ V - \sqrt{\frac{11\ \mu A}{(50\ \mu A/V^2)(1.3896)}} - |-0.85\ V| \\ V_{DS5}(sat) &\approx -0.0479\ V \end{aligned}$$

Applying Eq. (2.5), the aspect ratio of $M5$ is

$$\begin{aligned} S_5 &= \frac{2I_5}{K_5' \cdot V_{DS5}(sat)^2} \\ S_5 &= \frac{2(11\ \mu A)}{(50\ \mu A/V^2)(-0.0479\ V)^2} \\ S_5 &\approx 191.8717 \end{aligned}$$

Finally, to maintain the current flowing through $M5$ the same of the current source, the aspect ratio of transistor $M12$ is defined the same as $M5$, allowing *current mirroring* [2]. This is

$$S_{12} = S_5 \tag{4.20}$$

4.2.3 Current-Source Load Stage

The second stage of the OTA device permits a higher output swing in the amplifier. The parameters of this stage are defined below. By letting the second pole, p_2, to be at $2.2GB$, the transconductance of $M6$ is obtained as follows

$$g_{m6} = 2.2 g_{m2} \left(\frac{CL}{CC} \right) \tag{4.21}$$

To ensure a phase margin of at least 60°, the transconductance g_{m6}, must be greater or equal than $10g_{m1}$. Therefore, using Eq. (4.21) the value for g_{m6} is

$$\begin{aligned} g_{m6} &= 2.2(27.646\ \mu S)\left(\frac{10\ pF}{2.2\ pF} \right) \\ g_{m6} &\approx 276.46\ \mu S \end{aligned}$$

And since the phase margin condition is $g_{m6} \geq 10g_{m1}$ then

$$10g_{m1} = 10(27.646\ \mu S) = 276.46\ \mu S \tag{4.22}$$

Making $V_{SG4} = V_{SG6}$, the aspect ratio of device $M6$ is

$$S_6 = \frac{g_{m6}}{g_{m4}} S_4 \tag{4.23}$$

From Table 2.1 and Eq. (4.11), the transconductance of $M4$ is

$$g_{m4} \approx 12.222\ \mu S \tag{4.24}$$

Therefore, using Eq. (4.23) we obtain

$$\begin{aligned} S_6 &= \frac{276.46\ \mu S}{1.222\ \mu S}(0.1235) \\ S_6 &\approx 2.7925 \end{aligned}$$

The next step is to obtain the current flowing through $M6$. This could be either by transconductance or by current mirroring, as follows

a) By transconductance,

$$I_6 = \frac{g_{m6}^2}{2K_6' S_6} \tag{4.25}$$

$$I_6 = \frac{276.46\ \mu S}{2(110\ \mu A/V^2)(2.7925)}$$

$$I_6 \approx 124.41\ \mu A$$

b) By current mirroring, assuming $I_3 = I_4$ and from Eq. (4.7), $I_4 = 5.5\ \mu A$, therefore

$$I_6 = \frac{I_4}{S_4} S_6 \tag{4.26}$$

$$I_6 = \frac{5.5\ \mu A}{0.1235}(2.7925)$$

$$I_6 \approx 124.3623\ \mu A$$

Ideally, results from Eq. (4.25) and Eq. (4.26) must be equal. If they are not, as in this case, then the value obtained from transconductance of g_{m6} [Eq. (4.25)] should be the greater, otherwise a design trade-off will require to step back and change one specification.

The last transistor aspect ratio to be defined is S_7. Assuming

$$I_6 = I_7 \tag{4.27}$$

Then S_7 is

$$S_7 = \frac{I_7}{I_5} S_5 \tag{4.28}$$

Due to current mirroring I_5 through $M7$. The value for S_7 is

$$S_7 = \frac{124.41\ \mu A}{11\ \mu A}(191.8717)$$

$$S_7 \approx 2170.0178$$

Table 4.3 illustrates the transistor sizes for the circuit of Figure 4.2, which is the first design iteration. It is clear that those values are not valid for a CMOS IC design, however, they provide a good initial guess for the design methodology.

Table 4.3: Transistor sizes resulted from the first design iteration of OTA

Device	Ratio	Width [μm]	Length [μm]
M1	1.3896	1.3896	1
M2	1.3896	1.3896	1
M3	0.1235	0.12346	1
M4	0.1235	0.12346	1
M5	191.8717	191.87	1
M6	2.7925	2.7925	1
M7	2170.0178	2170.0	1
M12	191.8717	191.87	1

4.2.4 Requirements Comparison

To verify the theoretical performance of the OTA device, the numerical values of the established specifications compared against the information provided in Table 4.1.

Output Voltage Range

Given $V_{DS6}(sat) = V_{GS6} - V_{TN}$, from Table 2.1, we can obtain

$$\begin{aligned} V_{DS6}(sat) &= \frac{g_{m6}}{K'_6 S_6} \\ V_{DS6}(sat) &= \frac{276.46\ \mu S}{(110\ \mu A/V^2)(2.7925\ \mu m)} \\ V_{DS6}(sat) &\approx 0.9\ V \end{aligned} \tag{4.29}$$

The value for the minimum output voltage is given as

$$\begin{aligned} V_{GS6} &= V_{DS6}(sat) + V_{TN} \\ V_{GS6} &= 0.9\ V + 0.7\ V \\ V_{GS6} &= 1.6\ V \\ V_{OUT}(min) &= 1.6\ V \end{aligned} \tag{4.30}$$

From Eq. (4.27) and Eq. (2.5), the saturation voltage of $M7$ is given as

$$
\begin{aligned}
V_{SD7}(sat) &= \sqrt{\frac{2I_6}{K'_7 S_7}} \\
V_{SD7}(sat) &= \sqrt{\frac{2(124.41\ \mu A)}{(55\ \mu A/V^2)(2170.0178)}} \\
V_{SD7}(sat) &\approx 0.0479\ V
\end{aligned}
\tag{4.31}
$$

And the value for the maximum output voltage is

$$
\begin{aligned}
V_{OUT}(max) &= V_{DD} - V_{SD7}(sat) \\
V_{OUT}(max) &= 1.5\ V - 0.0479\ V \\
V_{OUT}(max) &= 1.4521\ V
\end{aligned}
\tag{4.32}
$$

From Table 4.1, the requirement for output voltage is defined as

$$-0.8\ V < V_{OUT} < 0.8\ V$$

And the output voltage range given by the first design iteration is

$$1.6\ V < V_{OUT} < 1.4521\ V$$

It is clear that there is a mistake due to nonvalid aspect ratios defined. Therefore, the specifications given in Table 4.1 need to be reviewed.

Power Consumption

The total power dissipation in the circuit of Figure 4.2 is

$$
\begin{aligned}
P_{diss} &= (V_{DD} + |V_{SS}|)(I_5 + I_6) \\
P_{diss} &= (1.5\ V + |-1.5\ V|)(11\ \mu A + 124.41\ \mu A) \\
P_{diss} &\approx 406.22\ \mu W
\end{aligned}
$$

Since the requirement establishes a $P_{diss} \leq 2$ mW, then this first design performs fine on power consumption.

Gain

From Eq. (2.32) the gain of the amplifier designed using the transistor sizes of Table 4.3 is

$$A_V = \left[\frac{2(27.646\ \mu S)}{11\ \mu A(0.04\ V^{-1}+0.05\ V^{-1})}\right]\left[\frac{(276.46\ \mu S)}{124.41\ \mu A(0.04\ V^{-1}+0.05\ V^{-1})}\right]$$

$$A_V \approx 1379.0256\ V/V$$

$$A_V(dB) = 20Log_{10}(1379.0256\ V/V) = 62.791\ dB$$

Table 4.1 shows that the minimum gain is

$$A_V = 2500\ V/V = 67.958\ dB$$

Therefore, the OTA gain does not meet the minimum requirement.

4.2.5 Right Half-Plane Zero Compensation

The undesired RHP zero may not be negligible in the design. This would occur if the GB specification is large or if the output stage transconductance, g_{m6}, is not big enough. Therefore, a nulling resistor is necessary to be placed right in series with the compensation capacitor to cancel the second pole, $p2$. The value of compensation resistor, Rz, should be

$$R_Z = \frac{1}{g_m 6}\left(\frac{CL+CC}{CC}\right) = \left(\frac{CL+CC}{CC}\right)\frac{1}{\sqrt{2K'_P S_6 I_6}} \tag{4.33}$$

The value of Rz from Eq. (4.33) for the circuit designed following the transistor sizes of Table 4.3 is

$$Rz \approx 20.059\ k\Omega \tag{4.34}$$

4.2.6 Iteration Process

Based on the methodology established on previous sections, an iterative process involving numerical approximations and computer simulations should be the next step in the OTA circuit design.

As mentioned before, the first iteration results are shown in Table 4.3. After several iterations, repeating design step calculations from 4.2.2 to 4.2.5, produces a higher gain OTA (see Figure 4.3). Appendix A includes a short list of the most relevant results from the numerical calculations procedure for designing a p-channel input two-stage OTA.

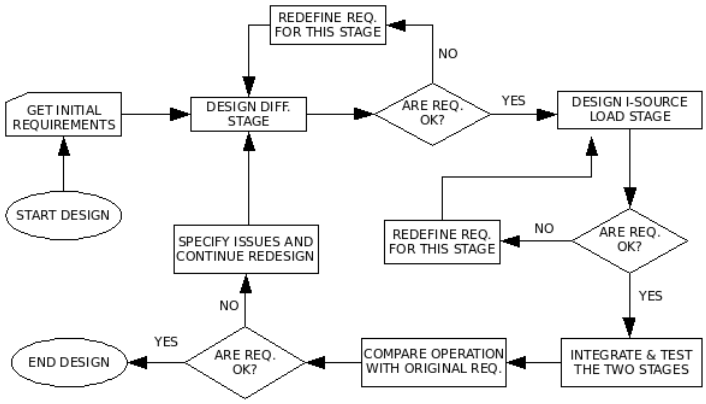

Figure 4.3: Flowchart diagram of the OTA design procedure.

During iterations, some dependencies can be deduced regarding to transistor aspect ratios and OTA gain. Gain increases when increasing the aspect ratio of the input pair, $M1$, $M2$, and by increasing their length as well. If the lengths of $M3$ and $M4$ are increased, the OTA gain also increases. Since transistor $M7$ is on the edge between nonsaturation and saturation region operation, by reducing aspect ratio S_7, transistor $M7$ goes through saturation operation, and OTA gain increases.

The aspect ratios of the new design, are shown on Table 4.4. The simulated gain is $A_V = 95.8519\ dB$. This circuit shows excellent gain and phase plots, which are illustrated in Figure 4.4. Moreover, the cut-off frequency is $f_{(-3dB)} = 134.42\ Hz$, and the unity-gain bandwidth is $GB = 6.4145\ MHz$, with a phase margin of $\Phi_M = 65.21821°$. However, we can observe from Figure 4.4 that the noise signal generated is considerable for analog applications [45], exceeding the typical tolerance for OTA circuits. The input noise voltage is low, $V_{INOISE} = 23.75\ nV^2/Hz$ at $1\ kHz$, but the output noise voltage is $V_{ONOISE} = 200\ \mu V^2/Hz$ at $1\ kHz$, which is a considerable magnitude [2].

Now, the transistor aspect ratios need to be modified in order to reduce the voltage gain to $A_V = 68dB$, which is the minimum design requirement. Noise effects are

Table 4.4: Transistor sizes of the two-stage CMOS OTA circuit with $A_V(dB) \approx 95.85\ dB$

Device	Ratio	Width [μm]	Length [μm]
M1	30	75	2.5
M2	30	75	2.5
M3	6	42	7
M4	6	42	7
M5	6.3	6.3	1
M6	30	15	0.5
M7	6.6	6.6	1
M12	6.3	6.3	1

reduced when reducing the gain.

By continuing iterating, the new aspect ratios defined for obtaining a voltage gain of $A_V = 68.11863\ dB$ with the circuit from Figure 4.2 are shown in Table 4.5.

Table 4.5: Transistor sizes of the two-stage CMOS OTA circuit with $A_V(dB) \approx 68\ dB$

Device	Ratio	Width [μm]	Length [μm]
M1	30	75	2.5
M2	30	75	2.5
M3	6	42	7
M4	6	42	7
M5	6.3	6.3	1
M6	30	15	0.5
M7	9.8	9.8	1
M12	6.3	6.3	1

This design has a noise output plot smaller than previous design, as it can be observed in Figure 4.5.

The cut-off frequency is $f_{V(-3dB)} = 2.835\ kHz$, and the unity-gain bandwidth is $GB = 6.92231\ MHz$, with a phase margin of $\Phi_M = 74.57352°$. Moreover, although input noise voltage maintains at $V_{INOISE} = 23.75\ nV^2/Hz$, now the output noise voltage reduces to $V_{ONOISE} = 50\ \mu V^2/Hz$.

As mentioned before, analog design is an iterative process, which involves several

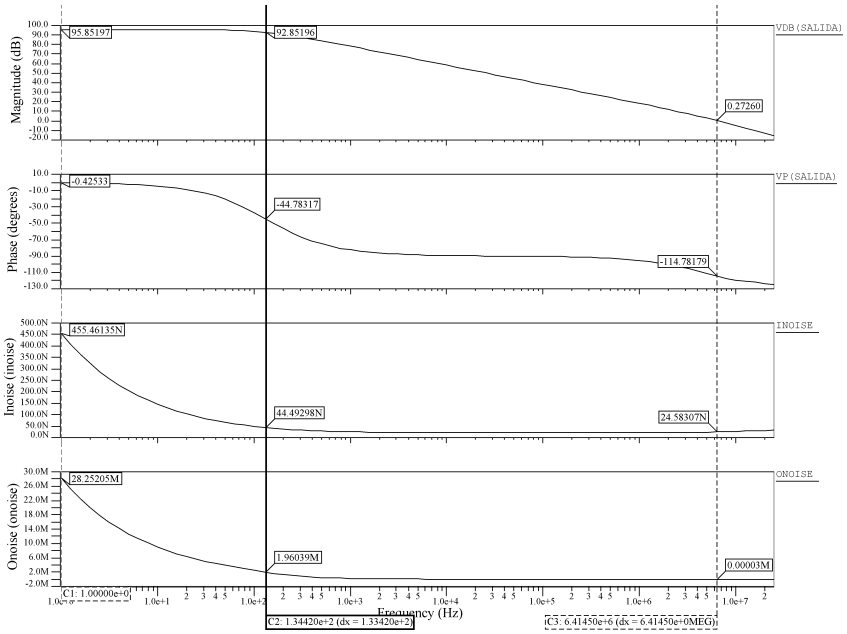

Figure 4.4: Frequency response of circuit with parameters from Table 4.4.

trade-offs and key decisions. If one single parameter is modified, the circuit operation changes, and to have better understanding of the circuit behavior, computer simulations are needed to analyze the design. Appendix B.1 includes a helpful Octave [46] script used in the numerical procedure to design a p-channel input two-stage OTA.

At this point, the aspect ratio of transistor $M7$ is the main parameter for controlling OTA's gain, because variations in width and length cause the device to operate either in the linear, or in the saturation region. This is, with parameters from Table 4.4 the circuit from Figure 4.2 achieves a voltage gain of $A_V \approx 95\ dB$. And when parameters from Table 4.5 are applied to the circuit shown in Figure 4.2, transistor $M7$ is forced to operate in the nonsaturation region, thus, the voltage gain is reduced to $A_V \approx 68\ dB$. Additional analysis and circuit simulations are discussed in Chapter 5.

4.2.7 Bias Voltage Circuit

Section 4.2.5 described the compensation of needed in the OTA device [1]. By including a resistor $R_Z \approx 20\ k\Omega$. In order to consider changing R_Z with a MOS device operating in the nonsaturation region, a bias voltage is needed to maintain this

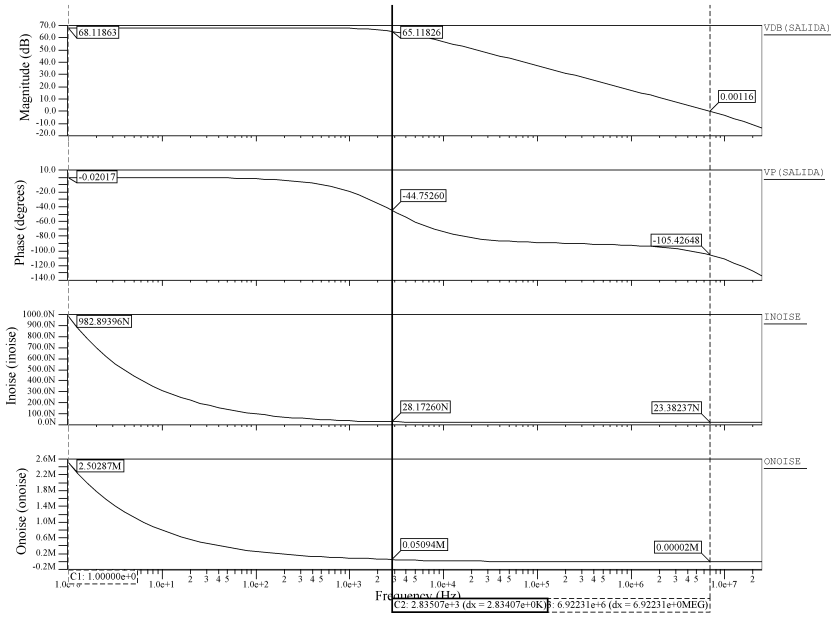

Figure 4.5: Frequency response of circuit with parameters from Table 4.5.

MOS transistor operating as a resistor. Considering the circuit shown in Figure 4.6, the methodology for defining the aspect ratios of transistors $M9$, $M10$, $M11$, $M12$ is resolved below.

First, a value for the current reference source, $IREF$, flowing through the new circuit block needs to be specified. Since Eqs. (4.6) and (4.20) define $I_5 = I_{12} = 11\ \mu A$, thus, an appropriate value for the current reference is selected as $IREF = 15\ \mu A$. Therefore, a good current value to bias the circuit is

$$I_{11} = I_{10} = I_9 = 5\ \mu A \tag{4.35}$$

Moreover, an arbitrary value for the aspect ratio of $M10$ needs to be defined. This is

$$S_{10} = 1 \tag{4.36}$$

Having these two parameters applied to Eq. (2.5), then

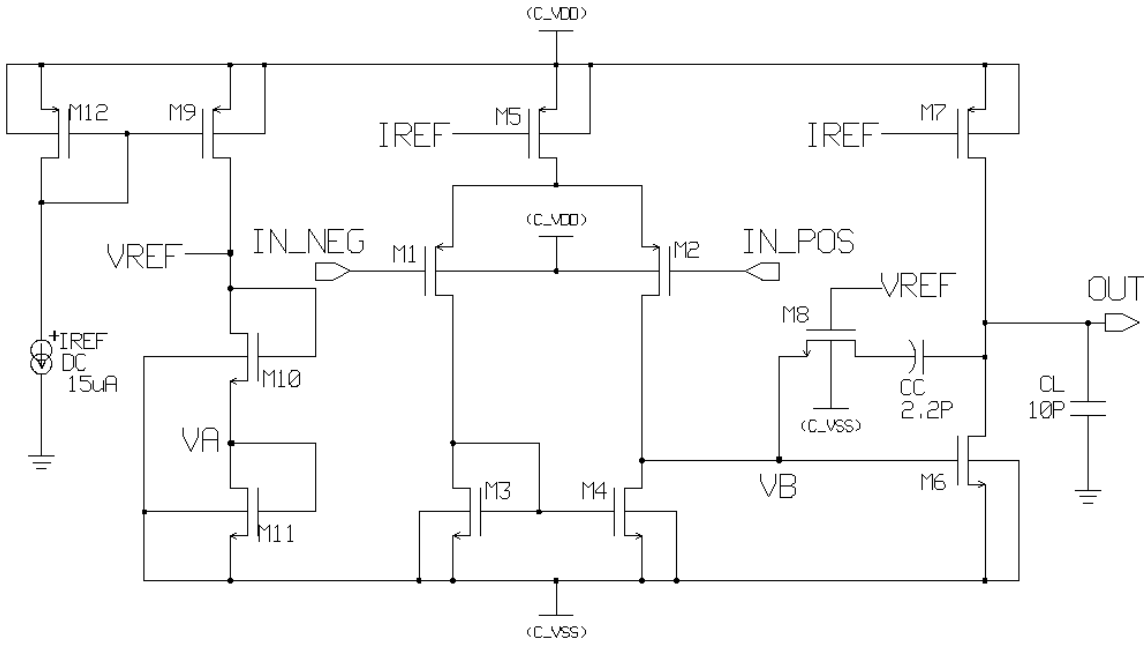

Figure 4.6: CMOS two-stage OTA using nulling resistor compensation.

$$
\begin{aligned}
V_{GS10} &= \sqrt{\frac{2I_{10}}{K'_{10}S_{10}}} + V_{T10} \qquad (4.37)\\
V_{GS10} &= \sqrt{\frac{2(5\ \mu A)}{(110\ \mu A/V^2)(1)}} + 0.7\ V\\
V_{GS10} &\approx 1.0015\ V
\end{aligned}
$$

According to Eq. (4.33), the compensation resistance is $R_Z = 20.059\ k\Omega$. Moreover, the bias circuit is designed so that (see Figure 4.6)

$$V_A = V_B \qquad (4.38)$$

As a result $V_{GS10} - V_{T10} = V_{GS8} - V_{T8}$. Considering this, by applying Eq. (2.7) the aspect ratio of $M8$ can be defined as

$$
\begin{aligned}
S_8 &= \frac{1}{K'_8 R_Z (V_{GS10} - V_{T10})} \\
S_8 &= \frac{1}{(110\ \mu A/V^2)(20.059\ k\Omega)(1.0015\ V - 0.7\ V)} \\
S_8 &\approx 1.5031
\end{aligned} \tag{4.39}
$$

To make calculations easier, the aspect ratio of $M8$ is changed to $S_8 = 1$. In order to comply with Eq. (4.38), $V_{GS10} = V_{GS6}$. Therefore, S_{11} can be obtained from

$$
S_{11} = \frac{S_6}{I_6} I_{11} \tag{4.40}
$$

Since the OTA should have a gain of $A_V = 68\ dB$, a recalculation of I_6 from Eq. (4.25), is needed, because $I_6 = 124.41\ \mu A$ produces a gain of $A_V = 95\ dB$. Therefore, the value for current of $M6$ at a total gain of $A_V = 68\ dB$ is equal to $I_6 = 27.5\ \mu A$, and the aspect ratio of $M6$ is obtained from Table 4.5. Thus Eq. (4.40) gives

$$
\begin{aligned}
S_{11} &= \frac{30}{27.5\mu A}(5\mu A) \\
S_{11} &\approx 5.4545
\end{aligned} \tag{4.41}
$$

The value of S_{11} is changed to $S_{11} = 5.5$ for practical considerations. Now, S_9 is defined as

$$
\begin{aligned}
S_9 &= \frac{S_5}{I_5} I_{10} \\
S_9 &= \frac{6.3}{11\ \mu A}(5\ \mu A) \\
S_9 &= 2.8636 \\
S_9 &\approx 2.85
\end{aligned} \tag{4.42}
$$

After several iterations on this stage, the optimum length values for the obtained aspect ratios are shown in Table 4.6.

Table 4.6: Transistor sizes of the bias voltage circuit

Device	Ratio	Width [μm]	Length [μm]
M8	1	0.5	0.5
M9	2.85	2.85	1
M10	1	0.5	0.5
M11	5.5	2.75	0.5
M12	6.3	6.3	1

Additional analysis and circuit simulations are discussed in Chapter 5. Appendix B.2 includes an Octave [46] script used for the iteration procedure.

4.2.8 Bias Current Circuit

An adequate current reference circuit is a very important functional block to bias current sinks and sources in the OTA device. If the reference circuit is designed properly, then the device could be used in portable systems. Figure 4.7 shows the current source topology used for designing this circuit stage. The MOS transistors $MC8$ and $MC7$, and the polysilicon resistance, $R\_START = 10\ k\Omega$, serve as the "start-up" circuit for the bias current circuit [2]; therefore, they are not needed when the load, $R1 = 200\ k\Omega$ is replaced by an active load. Once the bias current circuit module is integrated to the OTA circuit, the components $MC8$, $MC7$ and R_START can be removed from schematic.

Since the previously specified current for the circuit was $I_5 = 11\ \mu A$, the base current requirement selected is

$$IREF = 15\ \mu A \tag{4.43}$$

A slightly greater current is chosen in order to leave a margin of tolerance for the current source and being able to change any parameter as needed. By applying the *bootstrap reference* technique to the circuit from Figure 4.7, the equilibrium current is [2]

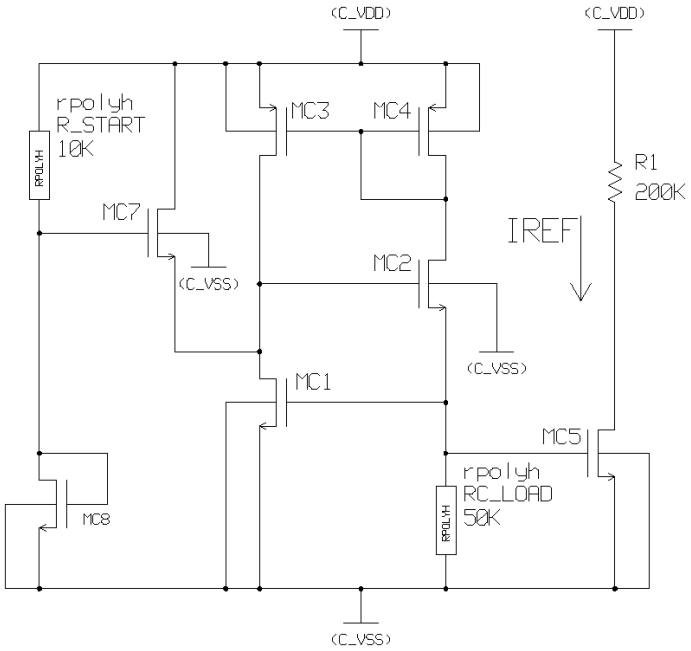

Figure 4.7: Bias current circuit.

$$IREF = I_{MC1} = I_{MC2} = \frac{V_{T\_MC1}}{RC\_LOAD} + \frac{L_{MC1}}{K'_{MC1} \cdot W_{MC1} \cdot RC\_LOAD^2} +$$

$$\frac{1}{RC\_LOAD}\sqrt{\frac{2 \cdot L_{MC1} \cdot V_{T\_MC1}}{K'_{MC1} \cdot W_{MC1} \cdot RC\_LOAD} + \frac{L_{MC1}^2}{{K'_{MC1}}^2 \cdot W_{MC1}^2 \cdot RC\_LOAD^2}} \quad (4.44)$$

Let us select RC_LOAD as follows

$$RC\_LOAD = 50\ k\Omega \quad (4.45)$$

From Eq. (4.44) the size of transistor $MC1$ is

$$W_{MC1} = 50\ \mu m \quad (4.46)$$

$$L_{MC1} = 0.5\ \mu m \quad (4.47)$$

Recalculating $IREF$ in Eq. (4.44)

$$IREF = \frac{0.7\ V}{50\ k\Omega} + \frac{0.5\ \mu m}{(110\ \mu A/V^2)(50\ \mu m)(50\ k\Omega)^2} +$$

$$\frac{1}{50\ k\Omega}\sqrt{\frac{2(0.5\ \mu m)(0.7\ v)}{(110\ \mu A/V^2)(50\ \mu m)(50\ k\Omega)} + \frac{(0.5\ \mu m)^2}{(110\ \mu A/V^2)^2(50\ \mu m)^2(50\ k\Omega)^2}}$$

$$IREF \approx 15.046\ \mu A \tag{4.48}$$

The next step in the procedure is to define a transistor MC_LOAD, that replaces RC_LOAD as shown in Figure 4.8. This is achieved by using the same methodology applied for replacing R_Z from section 4.2.7. The procedure initiates by recalling some of the calculations made for transistors $M10$ and $M11$ from Figure 4.6.

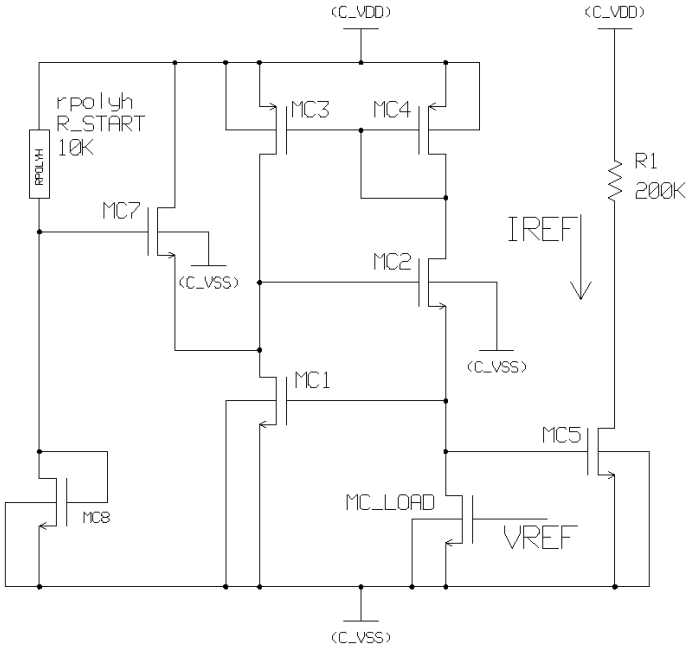

Figure 4.8: Bias current circuit with active resistance.

The V_{GS10} voltage for the MOS transistor $M10$, according to Eq. (4.37) was $V_{GS10} \approx 1.0015$ V. Also, according to Eq. (4.41), the aspect ratio for the MOS transistor $M11$ was $S_{11} \approx 5.4545$. Therefore, the V_{GS11} voltage, obtained from Eq. (2.5), is

$$
\begin{aligned}
V_{GS11} &= \sqrt{\frac{2I_{11}}{K'_{11}S_{11}}} + V_{T11} \\
V_{GS11} &= \sqrt{\frac{2(5\ \mu A)}{(110\ \mu A/V^2)(5.4545)}} + 0.7 \\
V_{GS11} &\approx 0.8291\ V
\end{aligned} \tag{4.49}
$$

The bias voltage of MOS transistor MC_LOAD is

$$
\begin{aligned}
V_{MC\_LOAD} &= V_{GS10} + V_{GS11} \\
V_{MC\_LOAD} &= 1.0015\ V + 0.8291\ V \\
V_{MC\_LOAD} &\approx 1.8306\ V
\end{aligned} \tag{4.50}
$$

Therefore, the aspect ratio of transistor MC_LOAD is

$$
\begin{aligned}
S_{MC\_LOAD} &= \frac{1}{K'_{MC\_LOAD}RC\_LOAD\{[V_{GS(MC\_LOAD)}] - [V_{T(MC\_LOAD)}]\}} \\
S_{MC\_LOAD} &= \frac{1}{(110\ \mu A/V^2)(50\ k\Omega)(1.8306\ V - 0.7\ V)} \\
S_{MC\_LOAD} &\approx 0.1608
\end{aligned} \tag{4.51}
$$

The best values for width and length of MC_LOAD are

$$
\frac{W_{MC\_LOAD}}{L_{MC\_LOAD}} = \frac{1.7\ \mu m}{11.2\ \mu m} = 0.15178 \tag{4.52}
$$

$$
\tag{4.53}
$$

The aspect ratios calculated for the circuit from Figure 4.8 are listed in Table 4.7.

Summarizing, the size of transistors defined for the final CMOS OTA design shown in Figure 4.9, are given in Tables 4.5, 4.6 and 4.7. Nevertheless, some final adjustments will be made to improve the matching characteristics of the layout. This is explained in Chapter 5.

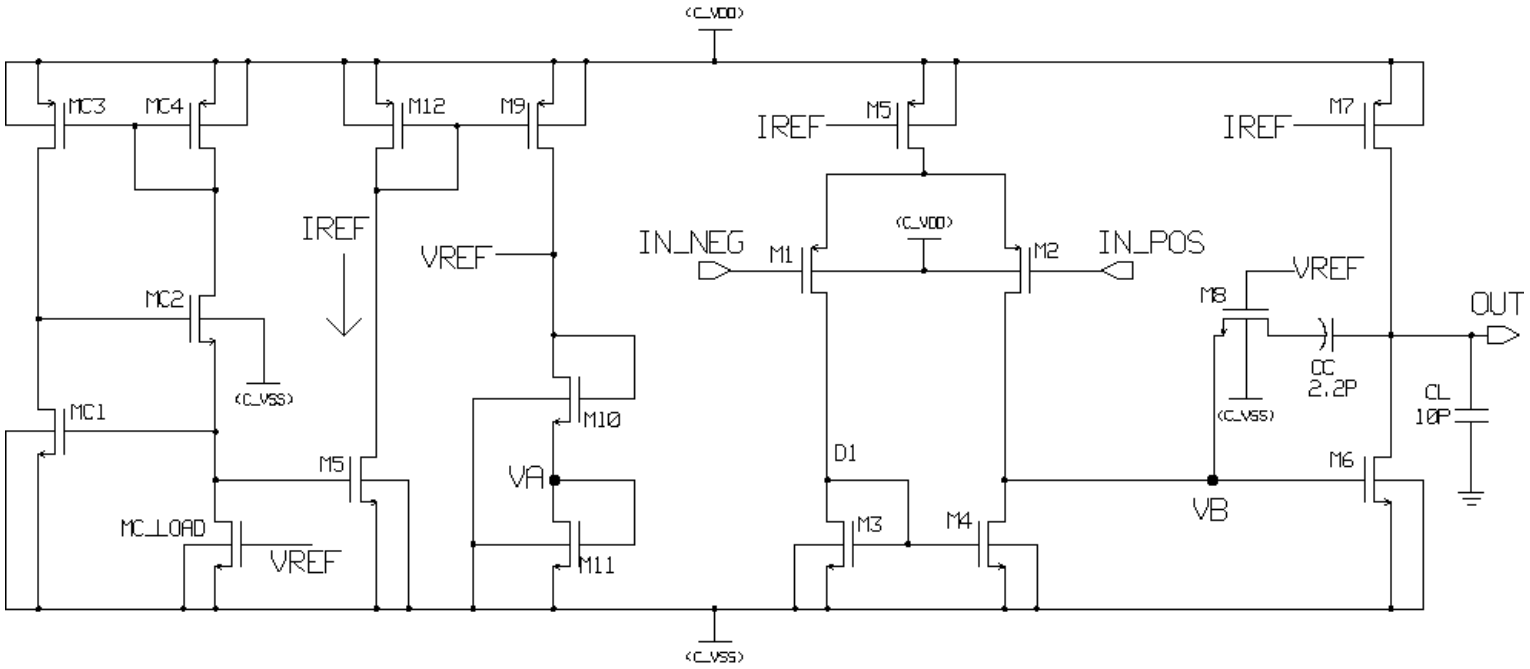

Figure 4.9: Complete two-stage CMOS OTA.

Table 4.7: Transistor sizes of the bias current circuit

Device	Ratio	Width [μm]	Length [μm]
MC1	100	50	0.5
MC2	100	50	0.5
MC3	100	50	0.5
MC4	100	50	0.5
MC5	100	50	0.5
MC_LOAD	1.7	11.2	0.151

4.2.9 System Modularization

A functional block implementation permits a modular structure and a well organized design. Therefore, splitting the OTA into individual functional blocks or modules provides a very flexible methodology to design complex microelectronics circuits. The modules integrate the design into functional blocks, which form a part of larger systems and a more complex device. Since modularization isolates circuit stages, it is easier to modify, find errors, or even replace complete circuit stages by just changing a single module. In Chapter 6, the layout of the system presents an improved modular design by applying this methodology. The following sections explain the way circuit modularization was performed for the OTA shown in Figure 4.9.

Differential Pair Circuit

The Figure 4.10 shows the differential amplifier input stage and Figure 4.11 shows its symbol.

Modified Differential Pair Circuit

In Chapter 6, the circuit configuration of the differential pair input stage will be changed for a double differential input stage in order to perform a *cross-quading*[1] design.

Cross-quading consists of common-centroid layout where each device is split in half and place diagonally opposite from each other. The diagonal transistors are connected

[1]Matching layout design technique for differential pair configuration.

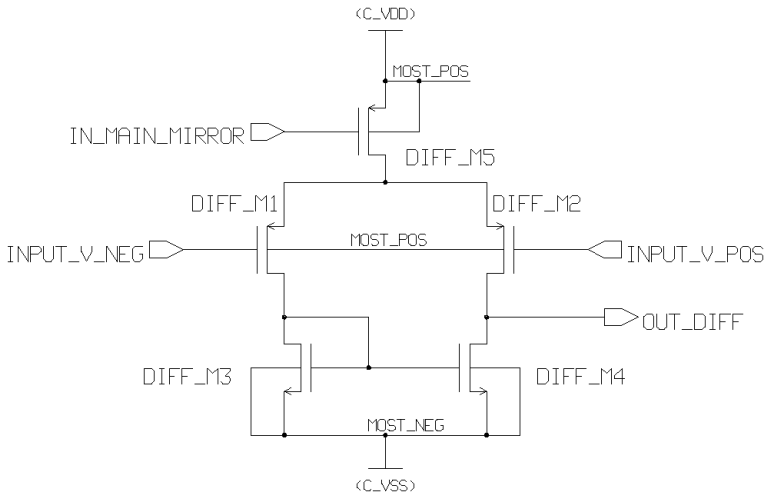

Figure 4.10: Differential pair schematic circuit diagram.

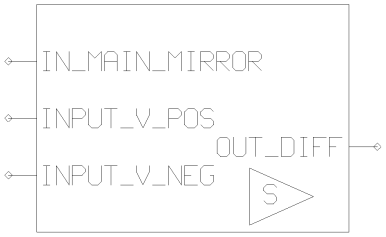

Figure 4.11: Differential pair symbol module.

in parallel, and operate as one single device. After applying cross-quading to a differential pair, four MOS devices at the input stage (operating as the original two-transistor pair) are now placed in the schematic circuit. This is to physically generate the layout of the input stage (composed now by four transistors), improving its matching and achieving temperature and current balance [23].

The final aspect ratios of the modified circuit stage are presented in Table 4.8. Also, the new schematic circuit diagram for the differential pair circuit and symbol are shown in Figures 4.12 and 4.13, respectively.

Table 4.8: Transistor sizes of the modified differential pair circuit

Device	Ratio	Width [μm]	Length [μm]
DIFF_M1	20	40	2
DIFF_M1_B	20	40	2
DIFF_M2	20	40	2
DIFF_M2_B	20	40	2
DIFF_M3	6	42	7
DIFF_M4	6	42	7
DIFF_M5	6.3	6.3	1

Current-Source Load Circuit

This stage requires special attention since it contains a capacitance, CC_1, made of two polysilicon layers. When the capacitance value is defined, ICstudio® calculates both, area and perimeter of the component. Because of its nature, capacitances require a lot of layout surface, which occupies the majority of the IC space. On this design, the defined value of $CC\_1 = 2.2\ pF$, requires an area of 2540.16 μm^2, and a perimeter of 201.6 μm for a square shape. Figures 4.14 and 4.15 show the current-source load schematic and symbol, respectively. Previously, Table 4.5 specified the sizes of the transistors for this module.

Bias Voltage Circuit

Figures 4.16 and 4.17 show the bias voltage schematic and symbol, respectively. Moreover, the Table 4.6 specified the sizes of the transistors for this module.

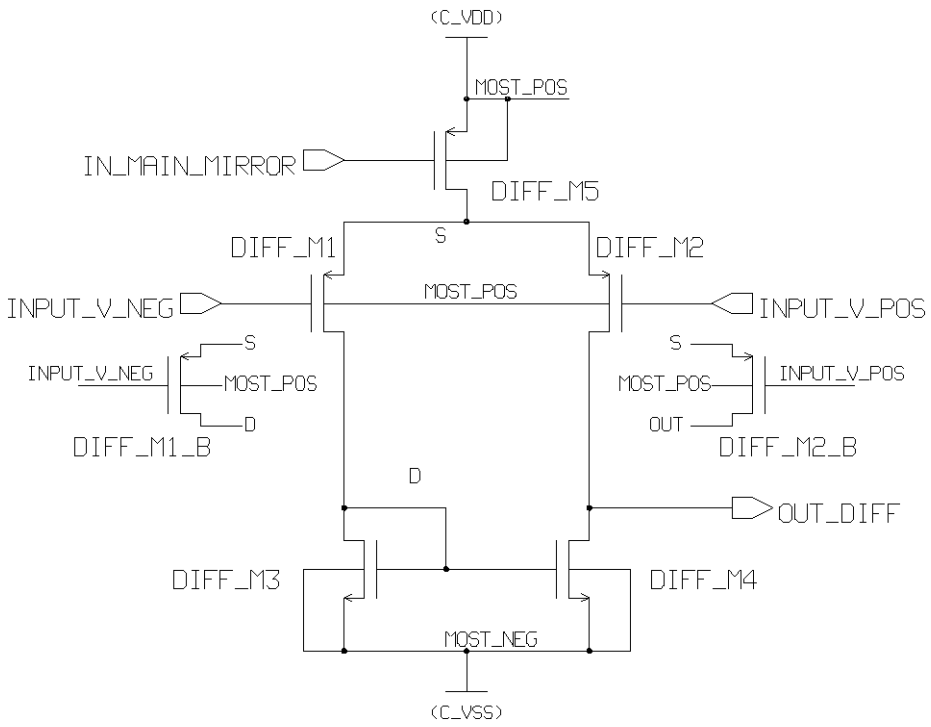

Figure 4.12: Modified Differential pair schematic circuit diagram.

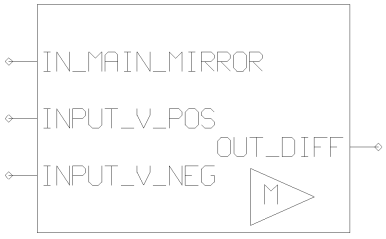

Figure 4.13: Modified Differential pair symbol module.

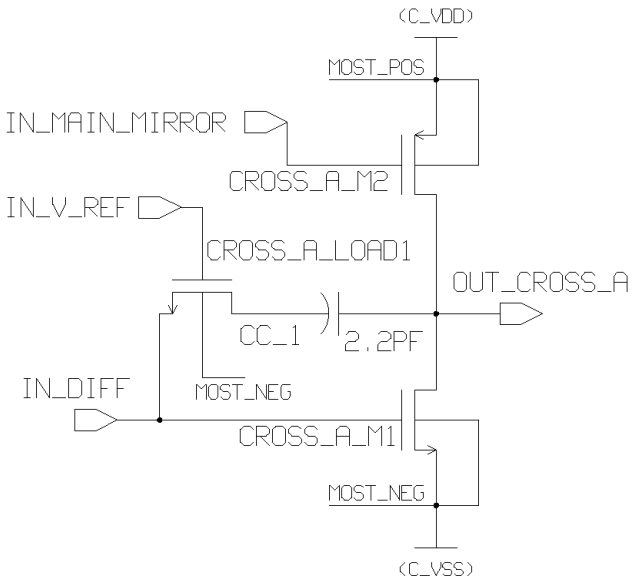

Figure 4.14: Current-source load schematic circuit diagram.

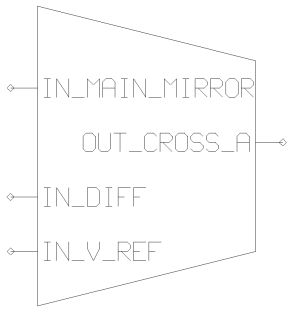

Figure 4.15: Current-source load symbol module.

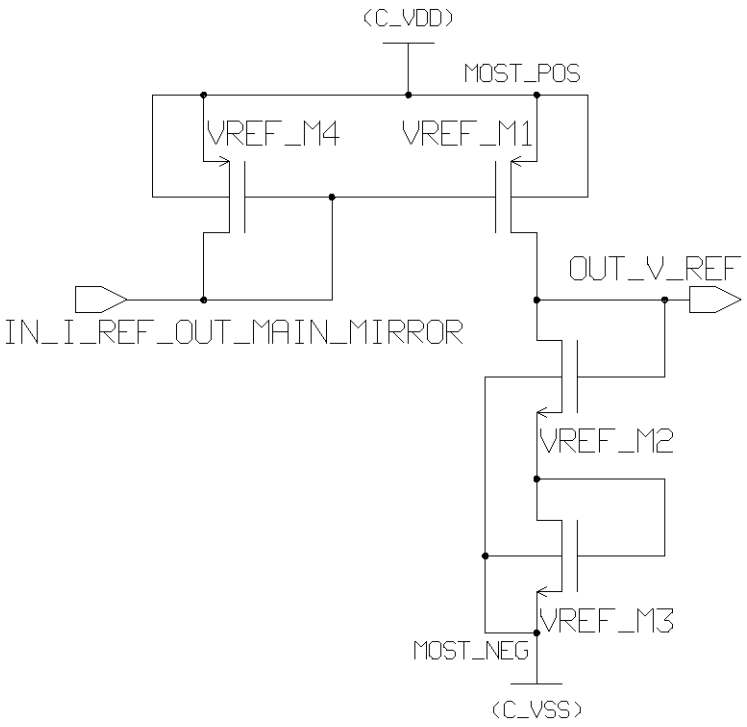

Figure 4.16: Bias voltage schematic circuit diagram.

Figure 4.17: Bias voltage symbol module.

Bias Current Circuit

Figures 4.18 and 4.19 show the bias current schematic circuit and symbol, respectively. Previously, the Table 4.7 specified the sizes of the transistors for this module.

4.2.10 OTA Packaging

The Figure 4.20 illustrates the modular structure presented in section 4.2.9, for the two-stage CMOS OTA circuit that was originally shown in Figure 4.9. Note that the modified differential pair circuit symbol module (see Figure 4.13) is now used. Moreover, the OTA overall schematic diagram is packaged into the symbol of Figure

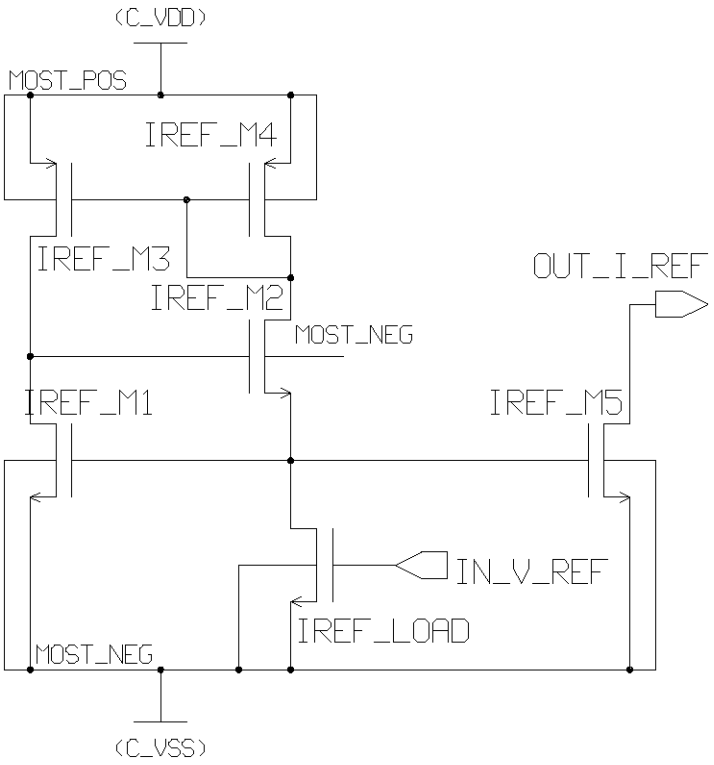

Figure 4.18: Bias current schematic circuit diagram.

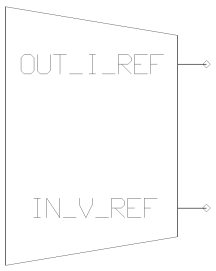

Figure 4.19: Bias current symbol.

4.21 to be used in the next hierarchical level.

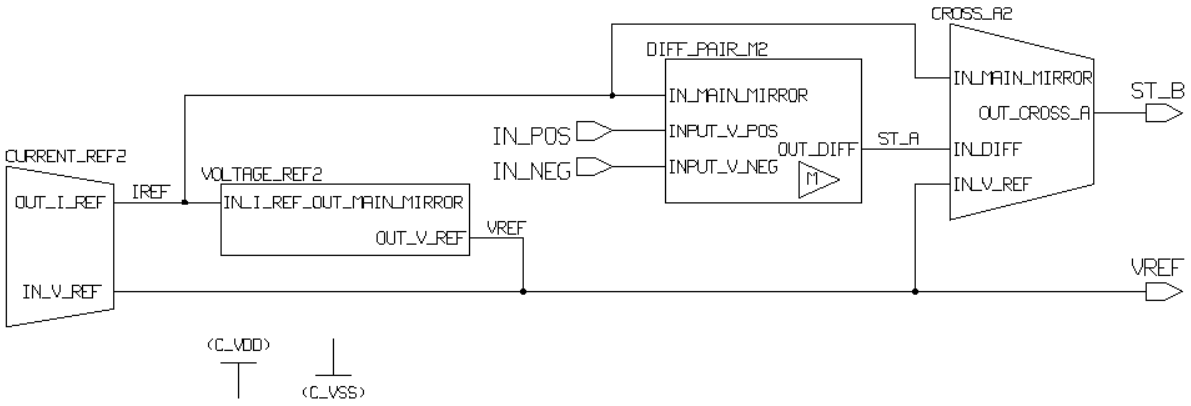

Figure 4.20: OTA schematic circuit diagram with bias output voltage connection.

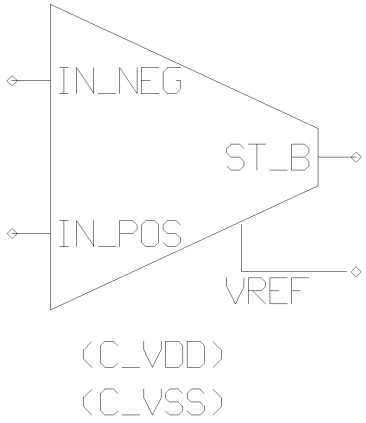

Figure 4.21: OTA symbol module with bias voltage output connection.

4.3 Instrumentation Amplifier

This section develops the design of an Instrumentation Amplifier (IA) [47] using the modular methodology. First, the gain requirement is satisfied by obtaining a consistent set of passive components. Then, the circuit implementation and verification are performed by substitution of active MOS transistors operating in the nonsaturation region instead of the calculated resistances. To consolidate the modular structure, a

new symbol is created for representing the instrumentation amplifier circuit to be used in a higher level hierarchical diagram.

4.3.1 Theoretical Design

The IA configuration is the *triple op-amp* implementation, and it is shown in Figure 4.22. The output gain of this circuit is

$$V_{OUT} = V_I \cdot \frac{R2}{R1}\left[1 + \frac{2R3}{R_G}\right] + V_{REF} \tag{4.54}$$

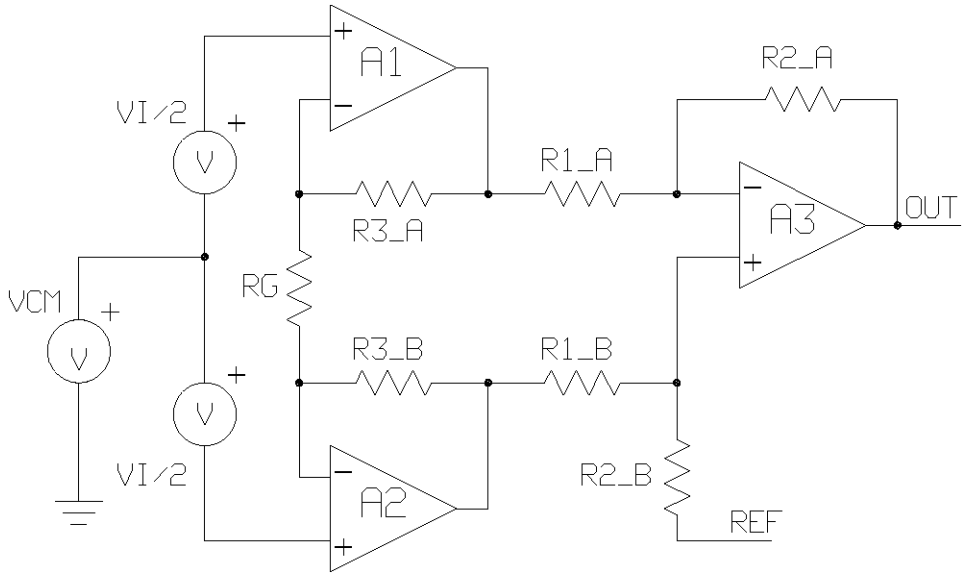

Figure 4.22: Triple op-amp IA circuit [8].

By establishing a voltage gain of $A_V = 100\ V/V$, a reference voltage of $V_{REF} = 0\ V$, the defined resistance values for circuit of Figure 4.22 are shown in Table 4.9. Therefore, according to Eq. (4.54) the theoretical gain value is given as

$$\begin{aligned} \frac{V_{OUT}}{V_I} &= \frac{100\ k\Omega}{100\ k\Omega}\left[1 + \frac{(2)(250\ k\Omega)}{5\ k\Omega}\right] \\ A_V &= 101\ V/V \end{aligned} \tag{4.55}$$

Table 4.9: Resistance values from the IA circuit.

Component	Value
R_G	5 kΩ
R1_A	100 kΩ
R1_B	100 kΩ
R2_A	100 kΩ
R2_B	100 kΩ
R3_A	250 kΩ
R3_B	250 kΩ

The high gain value of the first stage and the unity gain value of the second stage are selected to be $A_{VI} = 101$ and $A_{VII} = 1$, respectively, such that a high common-mode rejection ratio (CMRR) is obtained.

4.3.2 Practical Design

The final implementation of the IA developed in ICstudio® is shown in Figure 4.23. Note that the op-amp symbol corresponds to the two-stage CMOS OTA from Figure 4.21.

The magnitude vs. frequency response and the phase vs. frequency response obtained from simulating the circuit of Figure 4.23 are shown in Figure 4.24. The simulated gain of the circuit at a capacitive load of $C\_LOAD = 10$ pF is

$$\begin{aligned} A_V(dB) &= 40.00628\ dB \\ A_V &\approx 100.072\ V/V \end{aligned} \tag{4.56}$$

This result has a gain error of less than -1% with respect to the theoretical gain derived in Eq. (4.55), where ideal conditions were assumed [47].

4.3.3 Passive Components Replacement

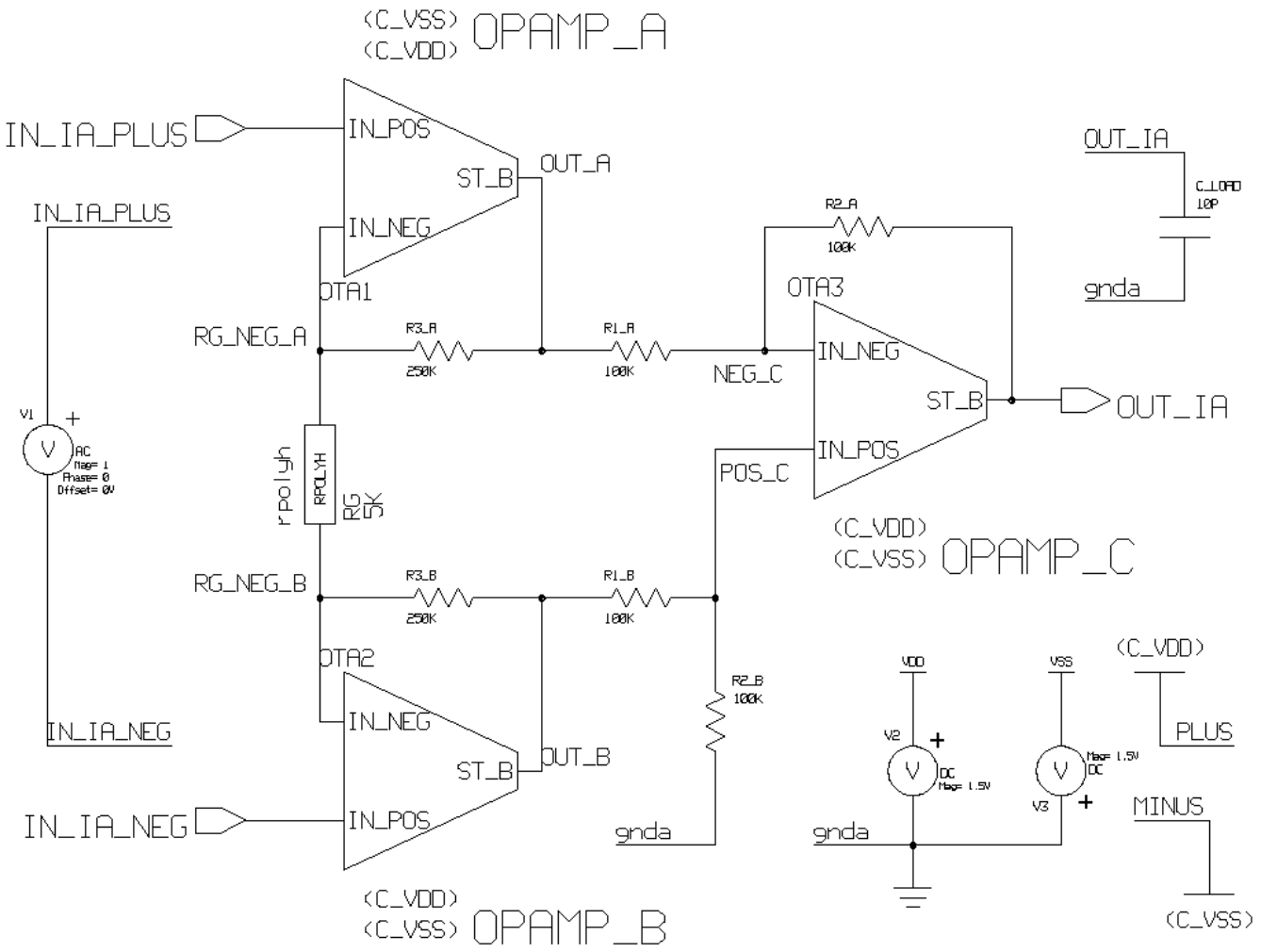

Figure 4.23: Design implementation of the IA with gain $A_V \approx 101$ V/V.

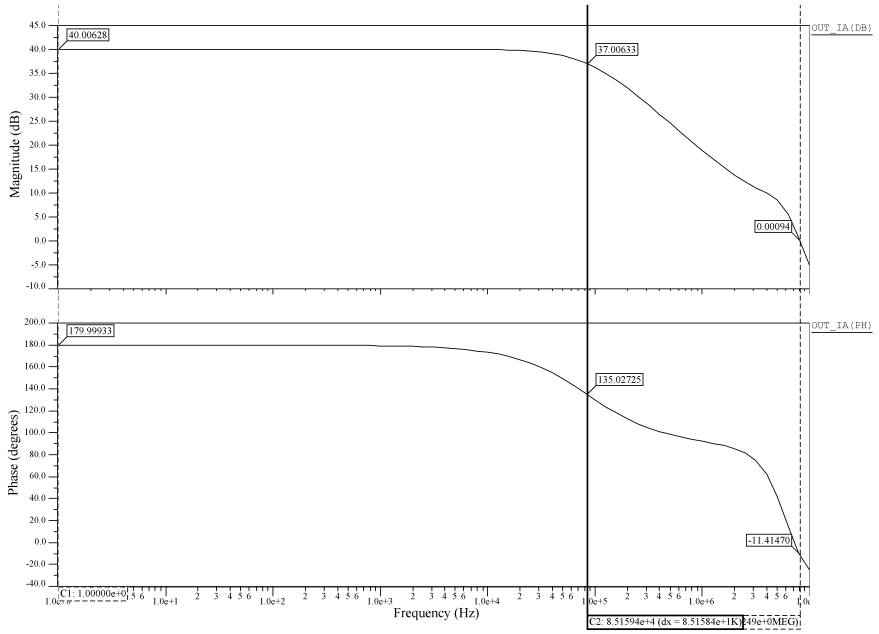

Figure 4.24: Frequency response of IA circuit from Figure 4.23.

Since silicon resistors require more surface space than MOS transistors, all resistances shown in the IA schematic are replaced by n-channel MOS transistors operating in the nonsaturation region. By using Eq. (2.7) and iterating with the simulation software tool, the required aspect ratios of transistors operating in the nonsaturation region are obtained and listed in Table 4.10.

The Figure 4.25 shows the modified schematic circuit with parameters from Table 4.10. The gain component, R_G, is implemented using a polysilicon resistor, to have the capability of changing the gain using a passive element.

Moreover, the Figure 4.26 illustrates the frequency response (in magnitude and phase) of the proposed IA design. The simulation results for a circuit gain are

$$\begin{aligned} A_V(dB) &= 40.60868\ dB \\ A_V &\approx 107.259\ V/V \end{aligned} \tag{4.57}$$

Since the theoretical gains provided by Eq. (4.55), Eq. (4.56) and Eq. (4.57) differ by at most 6.2 %, then the circuit has a very adequate performance for the intended application. Additional analysis and circuit simulations are discussed in Chapter 5.

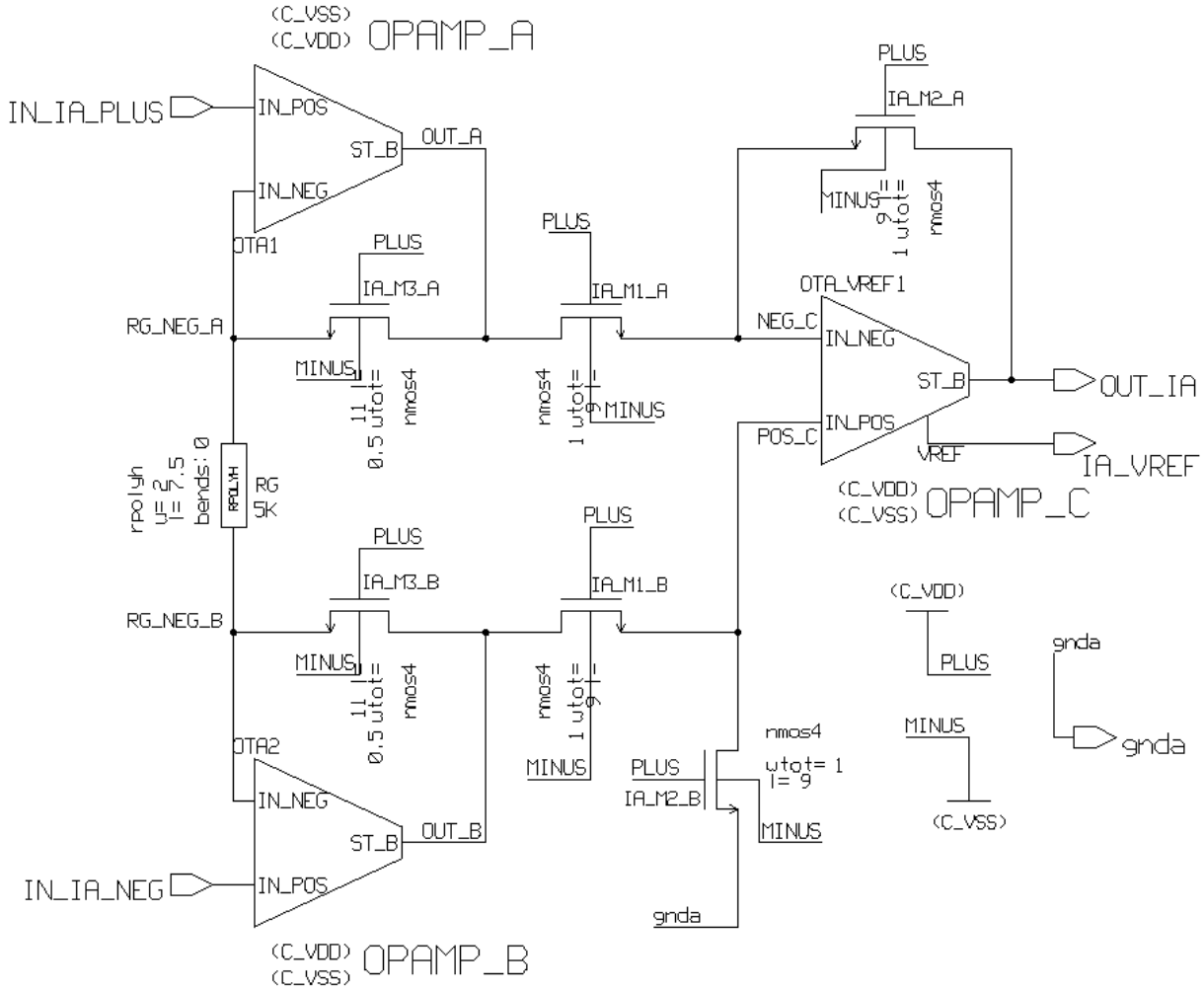

Figure 4.25: Modified IA schematic circuit diagram with reference voltage output connection.

Table 4.10: Transistor parameters for replacing resistances from circuit Figure 4.23

Passive component	Value	Active component	Width [μm]	Length [μm]	Gate voltage
R1_A	100 kΩ	IA_M1_A	1	9	V_{DD}
R1_B	100 kΩ	IA_M1_B	1	9	V_{DD}
R2_A	100 kΩ	IA_M2_A	1	9	V_{DD}
R2_B	100 kΩ	IA_M2_B	1	9	V_{DD}
R3_A	250 kΩ	IA_M3_A	0.5	11	V_{DD}
R3_B	250 kΩ	IA_M3_B	0.5	11	V_{DD}

4.3.4 IA Packaging

By following the modular device organization explained in section 4.2.9, the schematic diagram of the instrumentation amplifier appears in Figure 4.25. Moreover, the packaged five terminal symbol appears in Figure 4.27.

Note that the output port connection labeled as *gnda* will be the global analog ground. However, if the IA is used on a different application, the terminal port *gnda* could be connected to a required [8, 47].

4.4 Inverter Amplifier

This section discusses the design of the subsequent circuit stages of the signal conditioning system. A comparator is used to obtain a measurable squarewave signal. Therefore, a series of inverter amplifier circuits perform as a comparator amplifier. The procedure to design the comparator device consists of three phases as follows

a) To design a current-source inverter circuit,

b) to develop a triple push-pull inverter, and

c) To integrate the final circuit into a symbol.

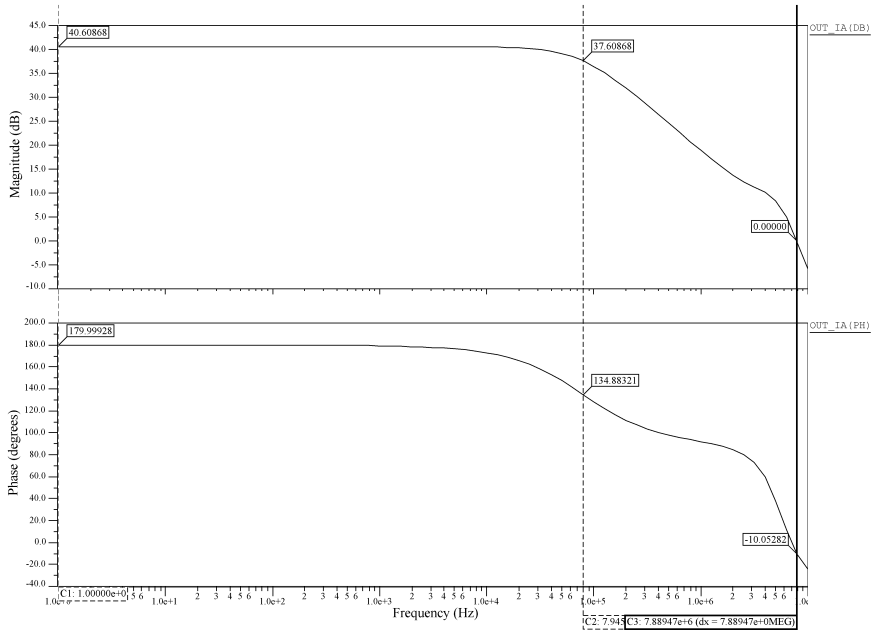

Figure 4.26: Frequency response of IA circuit from Figure 4.25.

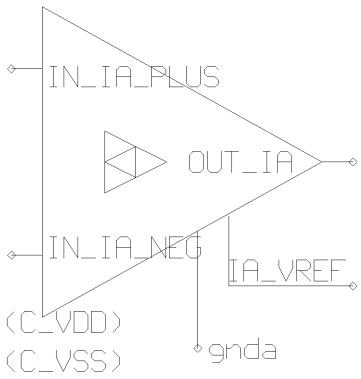

Figure 4.27: Five terminal instrumentation amplifier symbol module.

4.4.1 Current-Source Inverter Amplifier

The Figure 4.28 shows the schematic circuit of the current-source inverter amplifier. The p-channel transistor gate voltage is obtained from the bias voltage output of the previous circuit stage; therefore, $IN\_V\_REF \approx 186.89374\ mV$. A current of $I_D = 15\ muA$ is assumed in both transistors. Moreover, the n-channel MOS transistor size is defined as

$$S_n = \frac{W_n}{L_n} = \frac{2\ \mu m}{1\ \mu m} \tag{4.58}$$

The MOS transistor small-signal gain is

$$A_V = g_m \cdot R_{OUT} \tag{4.59}$$

And by using Eq. (2.17), the aspect ratio of the p-channel MOS transistor, for a gain of $\mathrm{A}_V = -30$ V/V, is given as [1]

$$\begin{aligned} S_p &= \frac{\left[A_V(\lambda_n + \lambda_p)\sqrt{\frac{I_D}{2}} - \sqrt{K'_n \cdot S_n}\right]^2}{\sqrt{K'_p}} \\ S_p &= \frac{\left[-30\ V/V \cdot (0.04\ V^{-1} + 0.05\ V^{-1})\sqrt{\frac{15\ \mu A}{2}} - \sqrt{110\ \mu A/V^2 \cdot 2\ V/V}\right]^2}{\sqrt{50\ \mu A/V^2}} \\ S_p &= 9.8805\ V/V \end{aligned} \tag{4.60}$$

If we assume a p-channel transistor length of $L_p = 1\ \mu m$, then, according to Eq. (4.60), the corresponding width is $W_p \approx 9.9\ \mu m$. After the first approximation of transistor sizes is known, an iterative methodology continues with circuit simulations. Then, the optimal transistor sizes for circuit of Figure 4.28 are obtained and listed in Table 4.11.

The VTC of the current-source inverter from Figure 4.28, with a load of $CL = 1\ pF$ and transistor sizes from Table 4.11, is shown in Figure 4.29. The graph shows that when $V_{IN} = -11.05\ mV$, the output is $V_{OUT} = 0\ mV$, thus the threshold voltage is $V_{th} = -11.05\ mV$. Therefore, this module presents an excellent performance, since $V_{th} \approx 0\ V$. The symbol module of this schematic circuit diagram is shown in Figure 4.30. Further analysis and circuit simulations are discussed in Chapter 5.

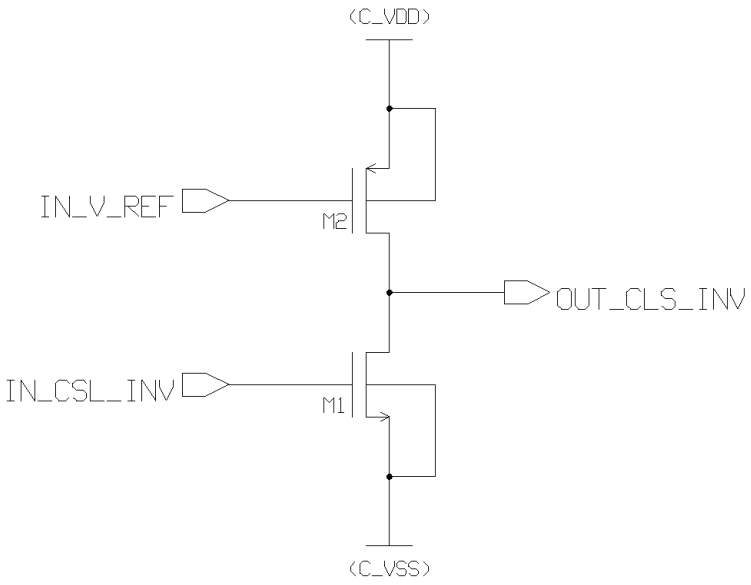

Figure 4.28: Current-source inverter schematic diagram.

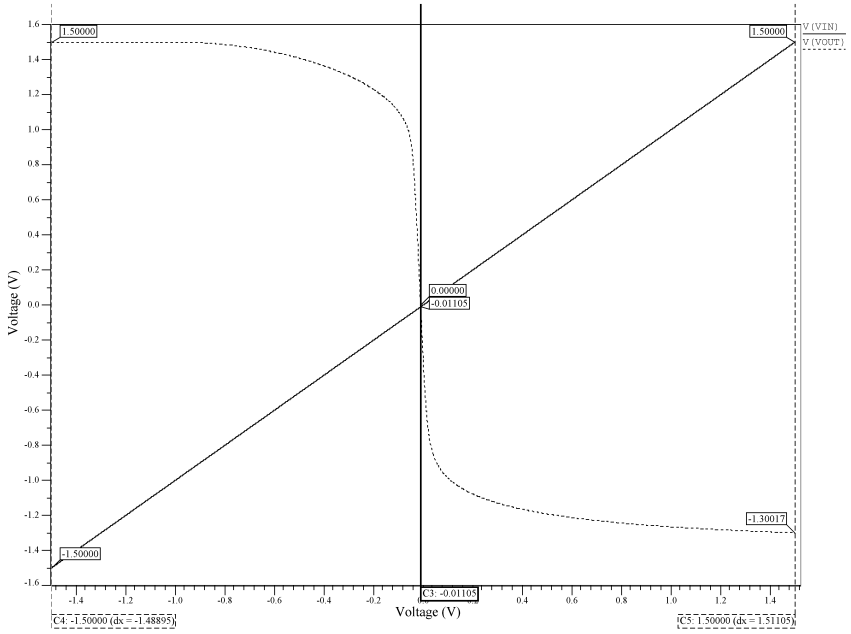

Figure 4.29: Voltage transfer curve of circuit Figure 4.28.

Table 4.11: Transistor sizes of current-source inverter circuit module

Label	Device	Ratio	Width [μm]	Length [μm]
M1	n-channel	1.65	1.65	1
M2	p-channel	10.15	10.15	1

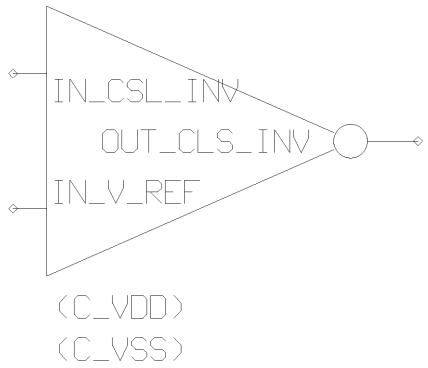

Figure 4.30: Current-source inverter symbol module.

4.4.2 Triple Push-Pull Inverter and Symbol Creation

When designing push-pull inverter amplifiers, a common approach is to specify the aspect ratio of both transistors, p-channel and n-channel, with identical values since ideal conditions are generally assumed for hand calculations. The next step is the iterative methodology using simulation tools until a satisfactory operation is achieved. Having the current-source inverter output signal to obtain a squarewave signal, three cascaded push-pull inverter stages are needed. The schematic circuit diagram of one single inverter module is shown in Figure 4.31 and the corresponding circuit symbol is shown in Figure 4.32.

The transistor sizes that conform the three stages are indicated in Table 4.12. Moreover, the VTC for inverter A, inverter B, and inverter C schematic circuits are shown in Figure 4.33, Figure 4.34, and Figure 4.35, respectively.

Figures show that the threshold voltages for each stage are $V_{th}(A) = -334.2\ mV$, $V_{th}(B) = -433.59\ mV$, $V_{th}(C) = 98\ \mu V$. These values were defined in order to obtain a low offset voltage on the final output signal. Further analysis and circuit simulations are discussed in Chapter 5.

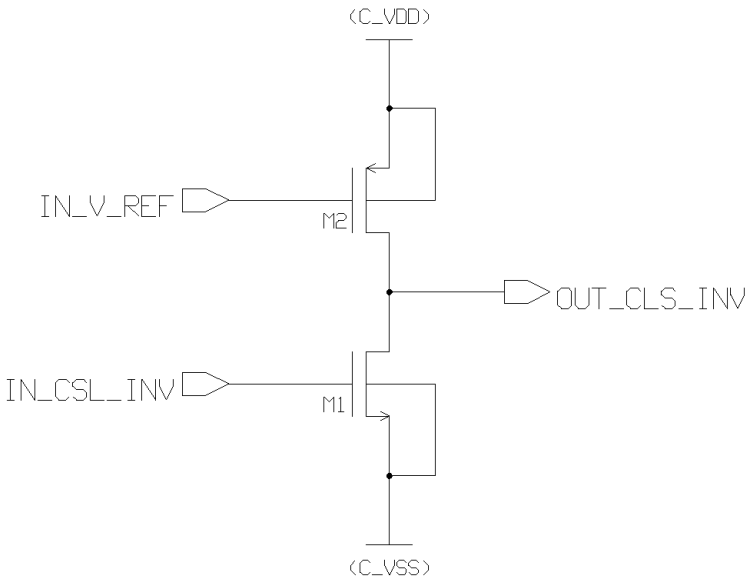

Figure 4.31: Schematic circuit diagram for inverter modules A, B, C.

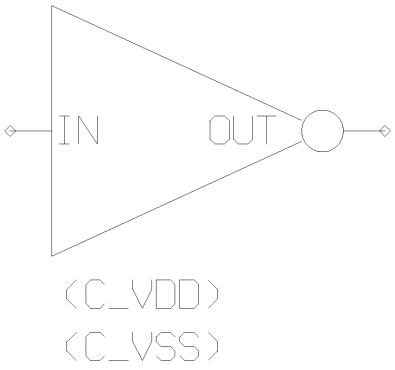

Figure 4.32: Individual symbol for inverter modules A, B, C.

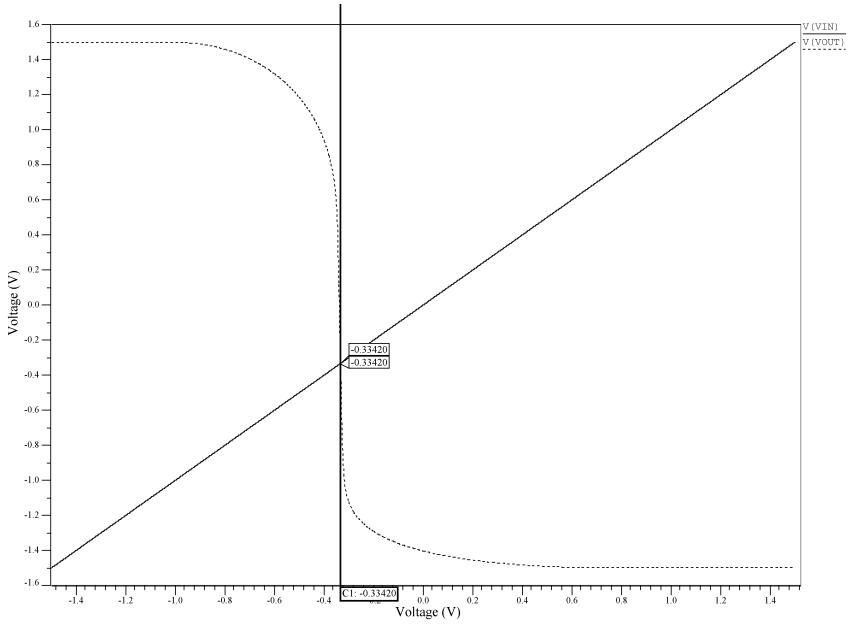

Figure 4.33: Voltage transfer curve of the push-pull A inverter amplifier.

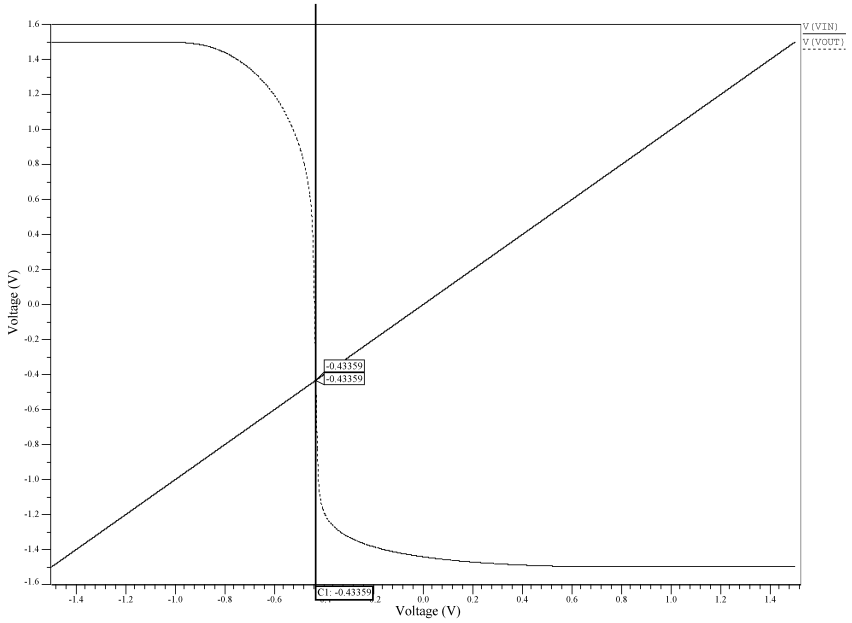

Figure 4.34: Voltage transfer curve of the push-pull B inverter amplifier.

Table 4.12: Transistor sizes of the three push-pull inverter circuit modules

Label	Device	Ratio	Width [μm]	Length [μm]
Inverter A	M1	1.05	1.05	1
	M2	1.1	1.1	1
Inverter B	M1	6	6	1
	M2	3.8	3.8	1
Inverter C	M1	1	1.2	1.2
	M2	4	4	1

A hierarchy schematic circuit diagram is developed from the push-pull inverter individual modules. The system is shown in Figure 4.36 and its symbol module in Figure 4.37.

4.5 Signal Conditioning Circuit

This section discusses the integration of the previous circuit modules in order to design a complete signal conditioning circuit for resonant MEMS sensors. First, circuits integration is explained, and second, the final circuit packaging for symbol generation is performed. As we mentioned before, further analysis and circuit simulations are covered in Chapter 5. Since a modular organization is followed through the circuit design, it is pretty simple to explain how the final schematic circuit is integrated.

4.5.1 Modules Integration

Integration of the signal conditioning circuit is done by connecting the IA of Figure 4.27, the current-source inverter of Figure 4.30, and the triple push-pull inverter of Figure 4.37. This results a system which schematic block diagram is posed in Figure 4.38.

4.5.2 Signal Conditioning Circuit Packaging

The Figure 4.38, shows a device which symbol generation option from ICstudio® results on the symbol shown in Figure 4.39.

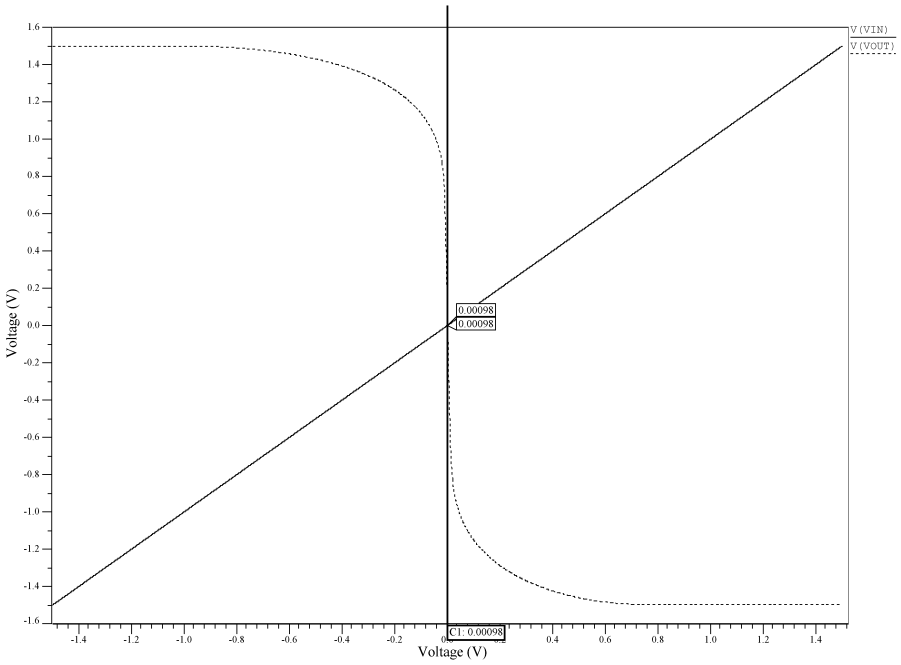

Figure 4.35: Voltage transfer curve of the push-pull C inverter amplifier.

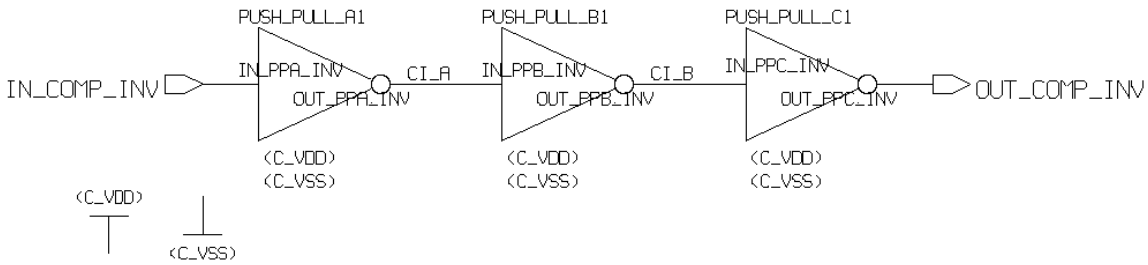

Figure 4.36: Triple inverter schematic circuit diagram.

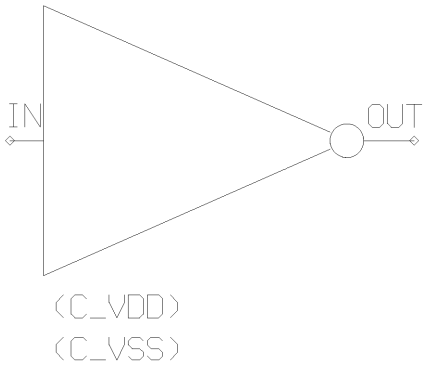

Figure 4.37: Triple inverter symbol module.

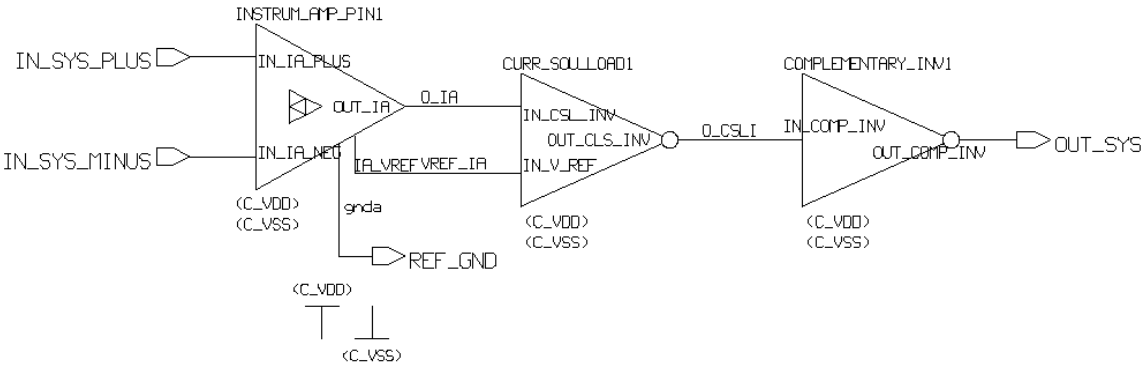

Figure 4.38: Signal conditioning circuit.

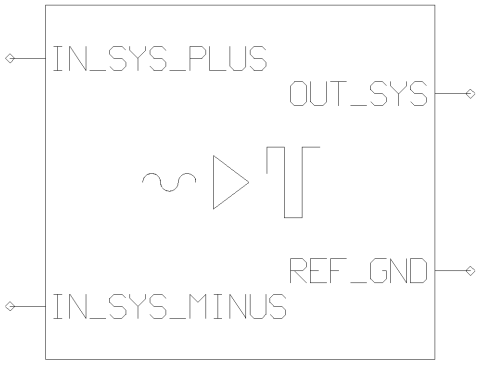

Figure 4.39: Signal conditioning circuit symbol.

Chapter 5

Circuit Simulation and Testing

5.1 Introduction

This chapter describes the simulation and testing of the electronic interface circuit designed by using ICstudio® tools and the AMS® 0.35μm technology. The simulation and testing includes the bias voltage source, the bias current source, and the operational transconductance amplifier. Moreover, the results include simulation outputs obtained from the instrumentation amplifier configuration and the triple-stage inverter circuit. Finally, the last section explains the integration and circuit simulation of the complete signal conditioning system.

5.2 OTA Simulation

The OTA circuit is simulated, first by testing its functional modules individually, and thenafter, by verifying the complete system performing all together. The simulation analysis performed to the functional modules are

a) Frequency domain analysis.

b) Voltage domain analysis.

c) Time domain analysis.

From those, the parameters such as settling time, output resistance, saturation voltages and power consumption, can be displayed or graphed using the Eldo® simulation tool [48].

5.2.1 Bias Voltage Circuit Time Response

By connecting the circuit symbol from Figure 4.17 as shown in Figure 5.1 (note that a load of $CL = 1\ pF$ is applied), the simulation results of Table 5.1 are obtained. The data shows that at a current source of $IREF = 15\ \mu A$, the node $VREF$ outputs a voltage of $VREF \approx 187\ mV$. Replacing the capacitive load by a resistive load of $RL = 47\ k\Omega$, the output voltage is reduced to the half, $VREF \approx 93.2\ mV$; thus, output resistance of this circuit stage is $R_{OUT} \approx 47k\Omega$. Since the $VREF$ terminal is connected to the gates of three MOS transistors, and a MOS gate terminal is theoretically an open circuit, then it is correct to assume that

$$R_{OUT} << RL \tag{5.1}$$

Therefore, applying a voltage divider

$$VREF = V_L = V_{OUT} \tag{5.2}$$

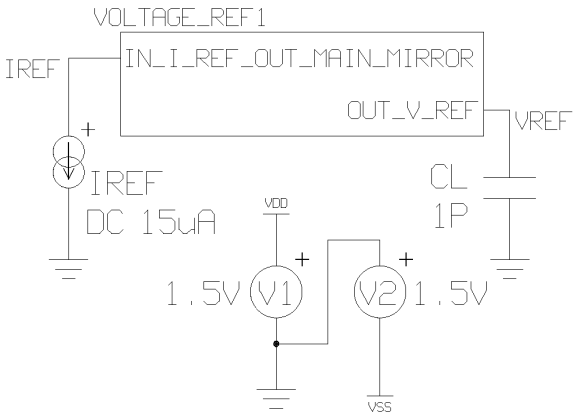

Figure 5.1: Circuit configuration for analysing the bias voltage module.

This output resistance value can be used as specification in case of being used for another application.

5.2.2 Bias Current Circuit Time Response

The Figure 5.2 shows a circuit to verify the operation of the bias current module. The plots obtained from simulations show that the circuit produces a current of

Table 5.1: DC operating point voltage of the bias voltage module at different loads

Load	DCOP Voltage
No load	187 mV
$CL = 1\ pF$	187 mV
$RL = 100\ k\Omega$	128.3 mV
$RL = 47\ k\Omega$	93.2 mV

$IREF \approx 15\ \mu A$ regardless of the resistive load, RL. According to results shown in Table 5.2, a variation on the load magnitude from $RL = 1\ \Omega$ to $RL = 70\ k\Omega$, causes a change on the current flow from $IREF = 17.2\ \mu A$ to $IREF = 14.99\ \mu A$, which is a very small variation compared to the variation on the applied load as shown

$$\Delta_{IREF} = 14.99\ \mu A - 17.2\ \mu A = -2.21\ \mu A \tag{5.3}$$

$$\Delta_{RL} = 70\ k\Omega - 1\ \Omega \approx 70\ k\Omega \tag{5.4}$$

$$\frac{\Delta_{IREF}}{\Delta_{RL}} = \frac{-2.21\ \mu A}{70\ k\Omega} = -31.57\ nA/k\Omega \tag{5.5}$$

The relation of current against resistive load indicates that there is a variation of $-31.57\ nA$ per $1\ k\Omega$ When the load is within a specified range, which is a very small variation. Therefore, the current $IREF$ is assumed to be independent of load resistance, if RL is within $1\ k\Omega < RL < 70\ k\Omega$, approximately. There is a $2.21\ \mu A$ variation, but considering that the load of the circuit is a MOS transistor operating in the saturation region (with a resistance of the order of $10\ k\Omega$), and the theoretical operating current is assumed at $I_5 = 11\ \mu A$ [see Eq. (4.6)], then the $IREF$ variation can be neglected.

The percent current regulation can be defined as

$$PIR = \frac{17.2\ \mu A - 14.99\ \mu A}{17.2\ \mu A} \times 100\ \%$$

$$PIR = 12.84\ \% \tag{5.6}$$

The value of $PIR = 12.84$ % is acceptable for the required aplication. Since transistor $M12$ is the device connected to the bias current circuit stage (see Figure 4.9), and there is assumed to operate in the saturation region, then the expected "on-resistance" for this transistor is on the order of $R_{M12}(on) \approx 10\ k\Omega$. Therefore, an $IREF$ magnitude slightly greater than the required value would be delivered for the bias current source circuit.

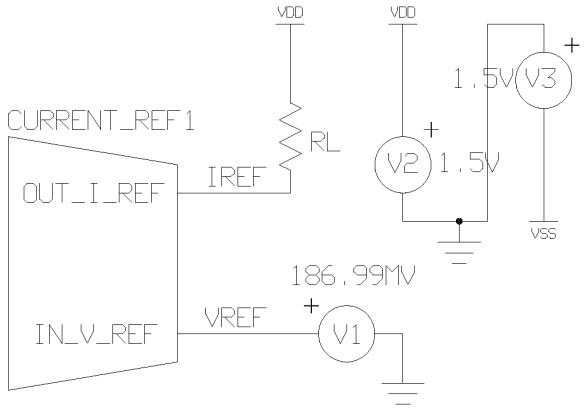

Figure 5.2: Circuit configuration for testing the bias current module.

Table 5.2: DC operating point voltage of the bias current module at different loads

Load	DCOP Current
$RL = 1\ \Omega$	17.2 μA
$RL = 100\ \Omega$	17.2 μA
$RL = 5\ k\Omega$	16.96 μA
$RL = 66\ k\Omega$	15.08 μA
$RL = 70\ k\Omega$	14.99 μA
$RL = 100\ k\Omega$	14.3 μA
$RL = 250\ k\Omega$	11.41 μA

5.2.3 OTA Frequency Response

The OTA represents the main circuit of the system. Having the OTA as the core of the device, the IA implementation consists of the integration of this reference module and passive components.

The *open-loop frequency response* simulation test is performed using the circuit shown in Figure 5.3. The circuit configuration measures gain and phase response for the OTA. An ac source, $V1$, is connected to the input terminals of the circuit module, and a capacitive load of $CL = 10\ pF$ is connected to the output terminal. Note that a load of $CREF = 1\ pF$ is connected to the $VREF$ output terminal. Figure 5.4 shows the simulation results for this open-loop frequency response simulation test.

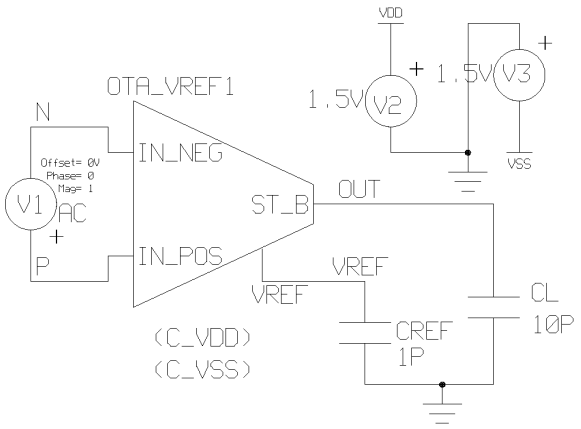

Figure 5.3: Circuit for testing the OTA's open-loop frequency response.

The Figure 5.4 illustrates that the OTA circuit has an open-loop gain of $A_V = 68.06558\ dB$, and the cut-off frequency is $f_{(-3dB)} = 2.93915\ kHz$. The unity-gain bandwidth is $GB = 7.06769\ MHz$, and the phase margin is $\Phi_M = 71.3157°$. This results are much better than the expected parameters shown in Table 4.1.

5.2.4 OTA Voltage Response

Circuit linearity is measured by replacing the ac voltage source (at the input terminals) by a dc voltage source. A voltage sweep of $-1.5\ V \leq V1 \leq 1.5\ V$ is applied to obtain the VTC shown in Figure 5.5. An excellent linearity is observed, and the measured offset voltage is $V_{OS} \approx 50\ \mu V$. Also, the saturation voltages are

$$V_{SS} \leq V_{OUT} \leq V_{DD} \tag{5.7}$$

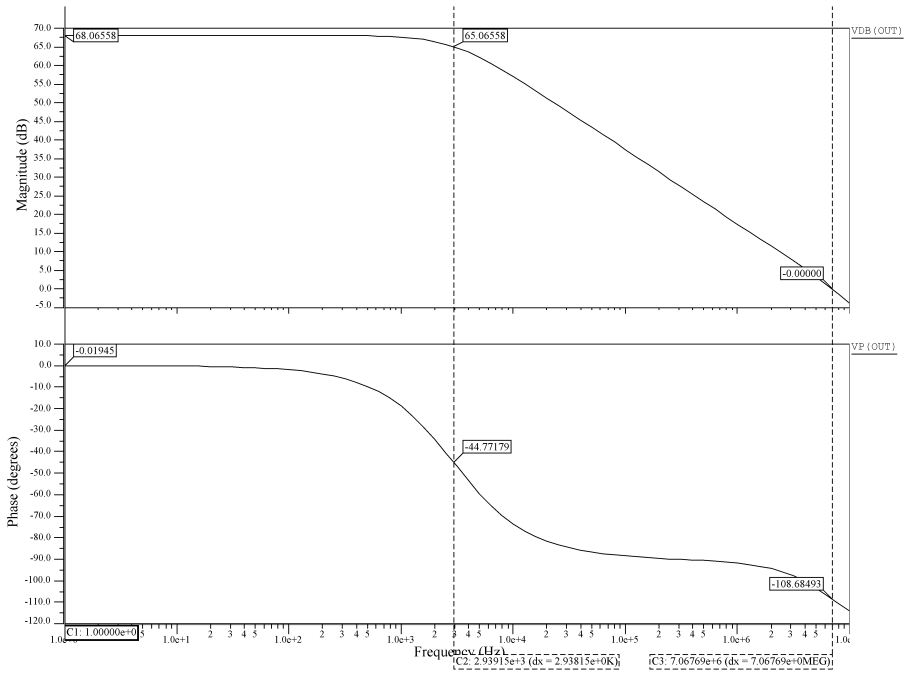

Figure 5.4: OTA's frequency response.

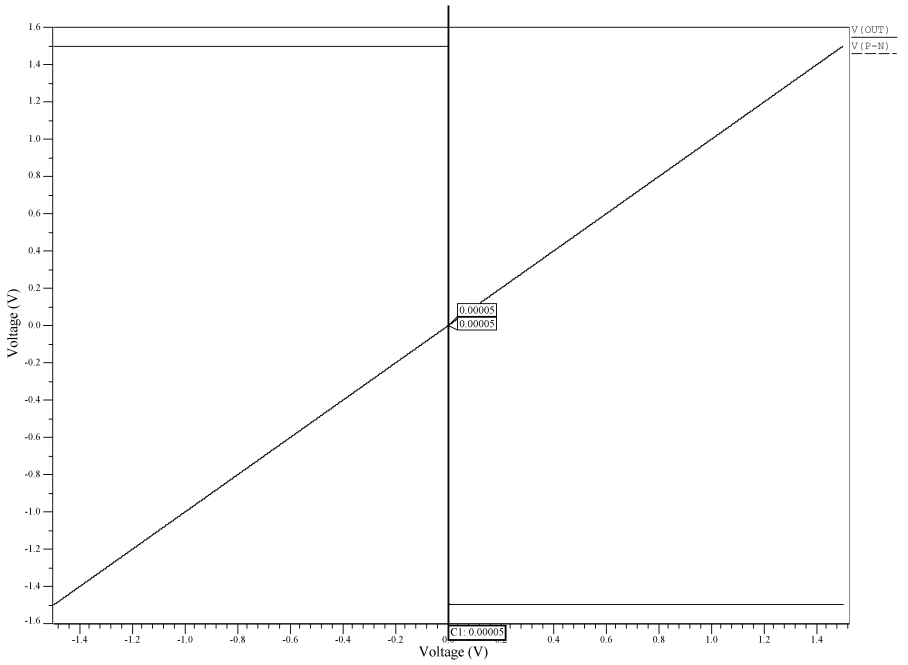

Figure 5.5: OTA's open-loop voltage transfer curve.

5.2.5 OTA Time Response

In order to measure circuit speed and settling time, a pulse voltage of $V_{PULSE} = 0.8\ V$ with a period of $T = 20\ \mu sec$ and a duty cycle of $DT = 50\ \%$ is used as the excitation voltage in circuit from Figure 5.6. The circuit is configured as a voltage buffer with a load of $CL = 1\ pF$, having a $t_d = 10\ \mu sec$ time delay for the pulse waveform. Figure 5.7 shows that the settling time for the rising edge is $t_{rise} = 1.65899\ \mu sec$, while the settling time for the falling edge is $t_{fall} = 499.82\ nsec$ (note that the input pulse signal starts falling at time $t = 20.001\ \mu sec$ due to a 1 $nsec$ falling time delay). The overshoot presented in the rising transition is due to the load capacitive effect, which decreases by reducing the original load capacitance of $CL = 10\ pF$ to the current value, $CL = 1\ pF$.

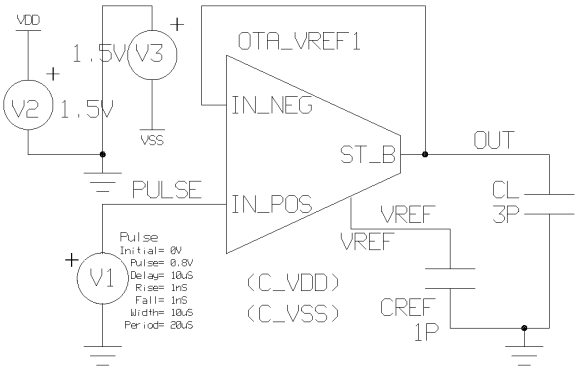

Figure 5.6: Circuit for testing the OTA's time response.

The slew rate measurement is performed by analyzing the rising edge output voltage from Figure 5.7. A closer view of the required signal segment is shown in Figure 5.8. Slew rate is defined from signal outputs at

$$\begin{aligned} t_1 &= 10\ \mu sec \\ t_2 &= 10.075\ \mu sec \end{aligned}$$

Defining the output voltages at t_1 and t_2

$$\begin{aligned} V_{OUT1} &= 53.44\ \mu V\ @\ t = t_1 \\ V_{OUT2} &= 594.86024\ mV\ @\ t = t_2 \end{aligned}$$

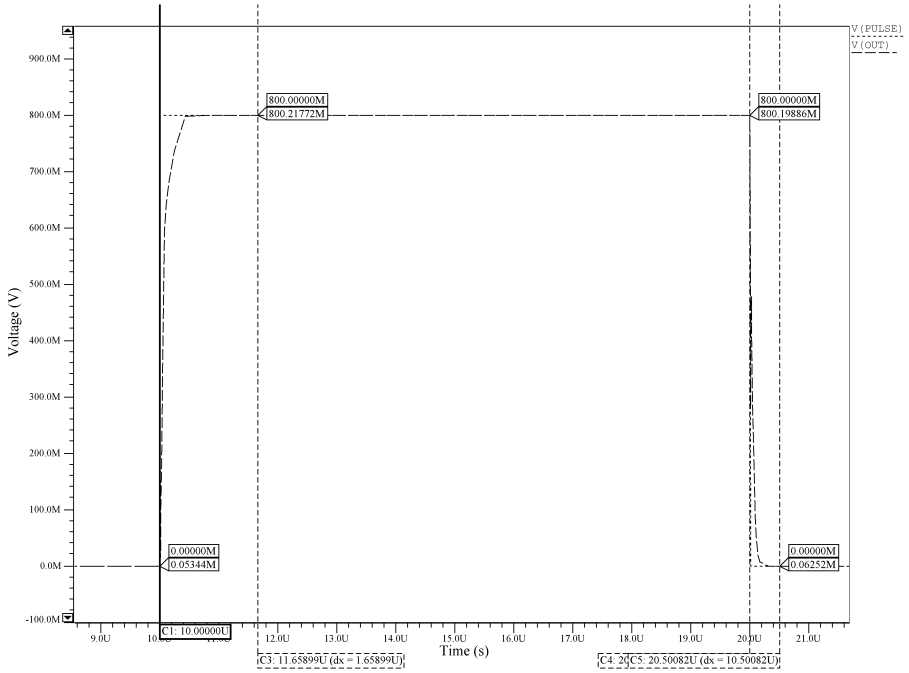

Figure 5.7: OTA's Time response.

Therefore, the positive transition slew rate, SR, is given as

$$SR = \frac{V_{OUT2} - V_{OUT1}}{t_2 - t_1} \tag{5.8}$$

$$SR = \frac{(594.86024 \times 10^{-3}\ V) - (53.44 \times 10^{-6}\ V)}{10.075\ \mu sec - 10\ \mu sec}$$

$$SR \approx 7.33\ V/\mu sec$$

The slew rate is better than the requirement from Table 4.1. However, as mentioned before, if the load capacitance increases, then the slew rate for the OTA decreases, due to the load capacitive effect.

5.3 Instrumentation Amplifier Simulation

This section describes the simulation analysis of the IA circuit. Frequency, voltage and time analysis are simulated and their results are explained.

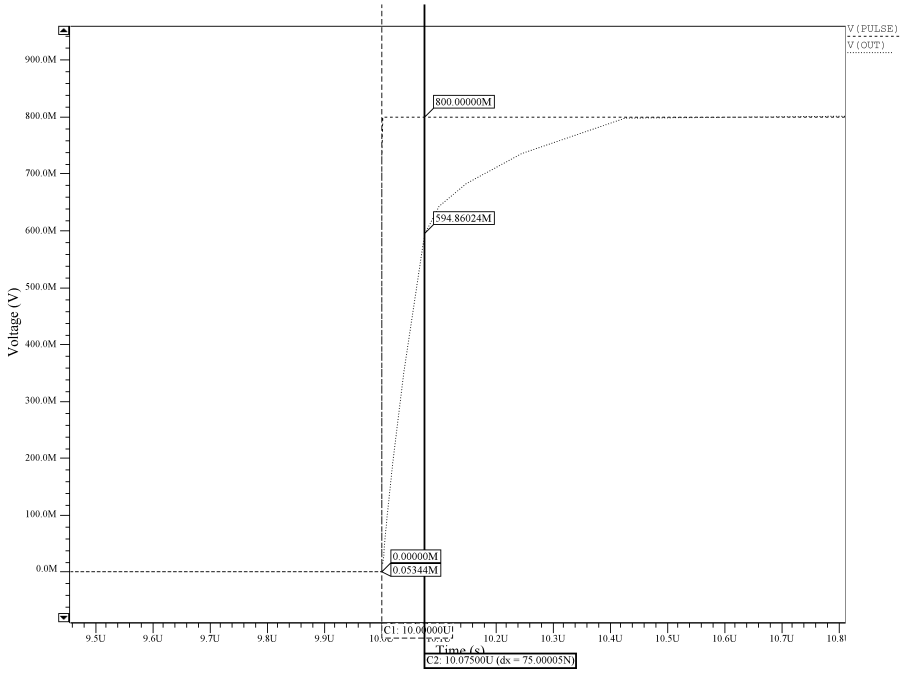

Figure 5.8: Closer view at the rising edge of OTA's time response.

5.3.1 IA Frequency Response

The frequency response of the IA can be simulated using the circuit of Figure 5.9. $V1$, is the input of the circuit, and a capacitive load of $CL = 10\ pF$ is connected at the output. Note that a load of $CREF = 1\ pF$ is also connected to the $VREF$ output terminal. Simulation results are shown in Figure 5.10.

According to plots, the gain of the IA is

$$\begin{aligned} A_V(dB) &= 40.60868\ dB \\ A_V &\approx 107.259\ V/V \end{aligned} \tag{5.9}$$

Moreover, the cut-off frequency is $f_{(-3dB)} = 79.4191\ kHz$. The unity-gain bandwidth is $GB = 8.88944\ MHz$, with a phase margin of $\Phi_M = 61.53267°$. The simulated gain is 6.2 % higher than theoretical gain, and cut-off frequency is twice the average resonant sensor frequency [26]. Therefore, the IA module meets the frequency operation requirements.

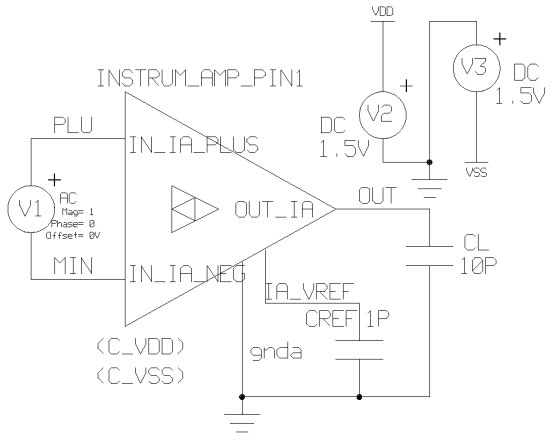

Figure 5.9: Circuit configuration for testing the IA's frequency response.

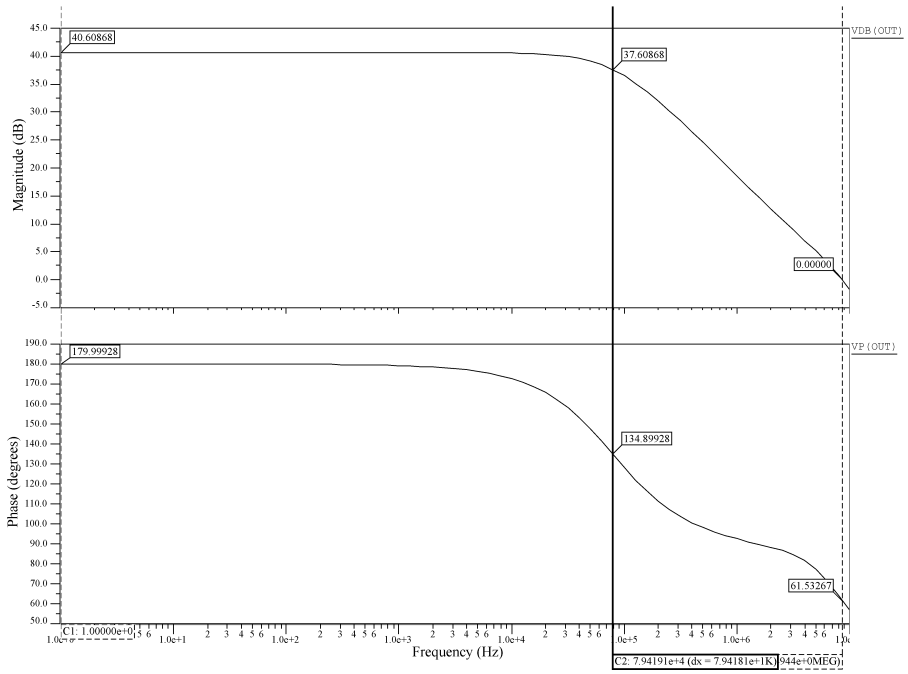

Figure 5.10: IA's Frequency response.

5.3.2 IA Voltage Response

The Figure 5.11 shows the circuit used to obtain the IA's VTC response. A capacitive load of $CL = 10\ pF$ is applied while performing a voltage sweep from $-1.5\ V \leq V1 \leq 1.5\ V$. The VTC appears in Figure 5.12. The results illustrate a very good linearity though the required operation range of $-100\ mV \leq V_{OUT} \leq 100\ mV$, and an offset voltage of $V_{OS} \approx 106.69\ \mu V$ (no indicated in plot, due to resolution). However, the graph also shows a nonlinearity at $V_{OUT} = -388.62\ mV$, which is caused by operating the transresistances in a dc analysis. The plot OUT_RES shows the behavior of the IA by using resistances instead of MOS transresistances, as in Figure 4.23. Therefore, the IA module will work properly for the required application.

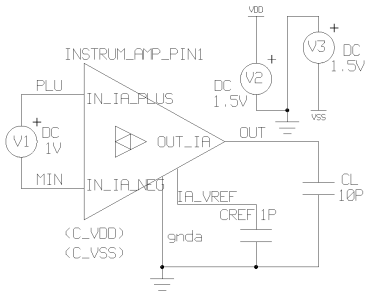

Figure 5.11: Circuit configuration for measuring the voltage transfer curve of the IA.

5.3.3 IA Time Response

The Figure 5.13 presents the required circuit configuration for performing a time analysis. A sinewave voltage source of $V1 = 1\ \mu V_P$ inputs the IA circuit module. If the input frequency is higher than the cut-off frequency, previously indicated as $f_{(-3dB)} = 79.4191\ kHz$, then the output signal decreases proportional to the plot from Figure 5.10.

Figure 5.14 shows the differential input and single output of the circuit from Figure 5.13 with an input signal frequency of $f = 10\ kHz$. As expected, the output voltage magnitude is near to

$$V_{OUT} \approx [A_V \cdot V_{(P-N)}] + V_{OS} \tag{5.10}$$

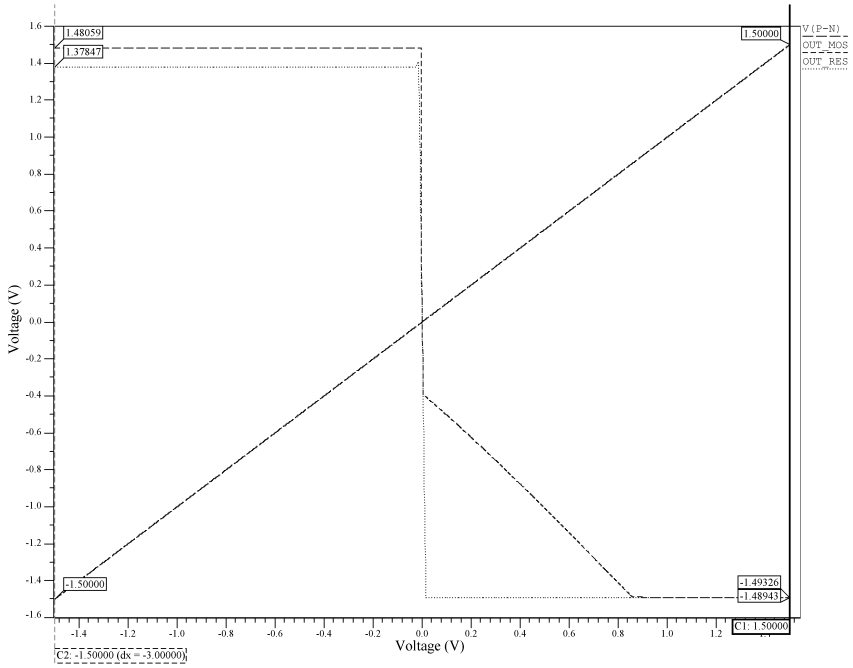

Figure 5.12: Voltage transfer curve from circuit of Figure 5.11.

Where $V_{OS} \approx 106.69\ \mu V$, is the offset voltage. Therefore, when $V_{(P-N)} = 1\ \mu V$, the output signal, V_{OUT} , is approximately 6.2 % greater than theoretical design.

In contrast, Figure 5.15, obtained from a 100 kHz sine voltage source of 1 μV of amplitude, shows a lower gain compared to Figure 5.14, and a notable phase shift, which affects the performance of the other circuit modules.

5.4 Inverter Amplifier Module Simulation

As in previous sections, to verify the proper operation of the inverter circuits, the individual modules were analyzed. Once this test was finished, a simulation of the whole system, completes the validation. Th purpose of the inverter module stages is to compensate the offset voltage from previous stages and to saturate the input signal, in order to obtain a squarewave signal with its frequency proportional to the original signal frequency.

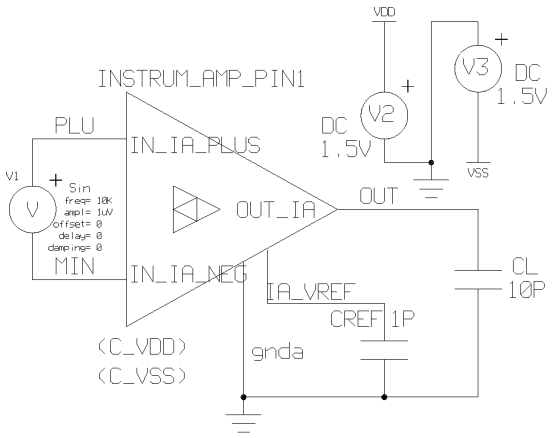

Figure 5.13: Circuit configuration for testing the time response of the IA.

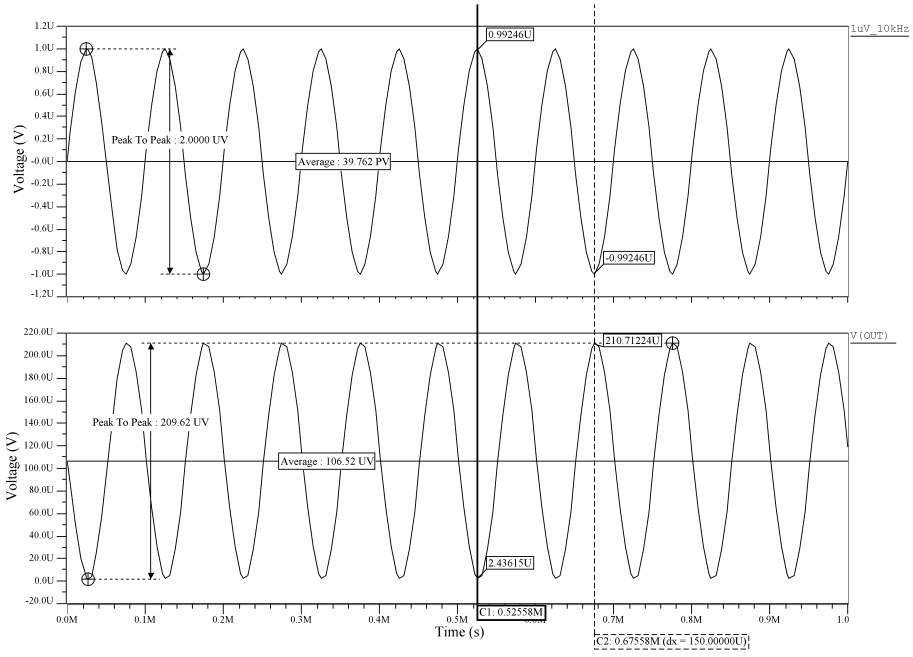

Figure 5.14: Time response from circuit of Figure 5.13 at $f = 10\ kHz$.

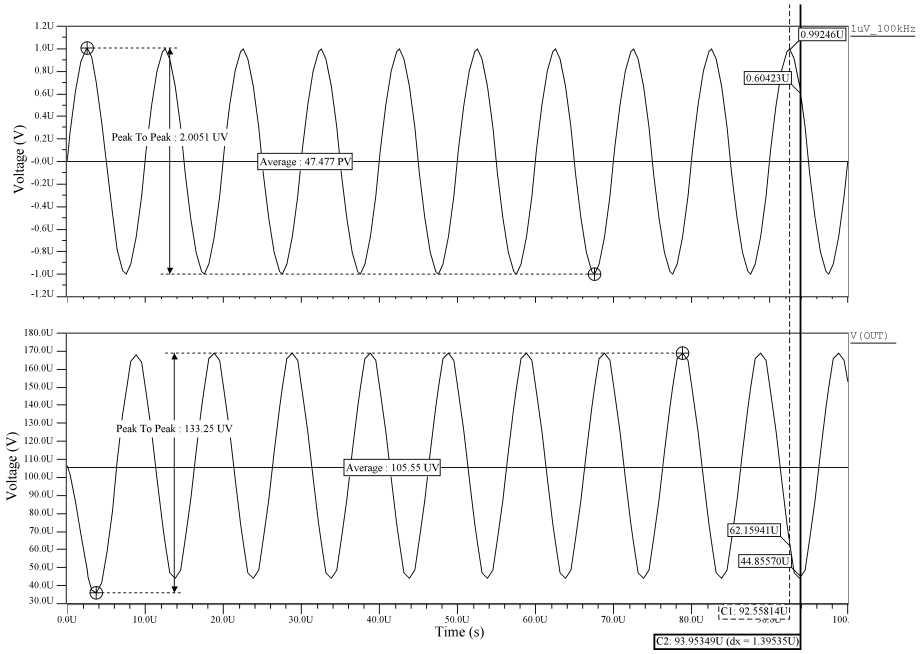

Figure 5.15: Time response from circuit of Figure 5.13 at $f = 100\ kHz$.

5.4.1 Current-Source Inverter Frequency Response

The figure 5.16 shows the circuit to measure the gain of the current-source inverter module. An ac source, $V1$, is connected to the input terminals of the circuit, and a capacitive load of $CL = 1\ pF$ is connected to the output terminal. A voltage of $VREF = 186.89374\ mV$ is used to maintain a stable current source, and the simulation results are shown in Figure 5.17.

The inverter gain obtained from simulation is $A_V = 28.813\ dB = 27.586\ V/V$, and the cut-off frequency is $f_{(-3dB)} = 803.536\ kHz$. The unity-gain bandwidth is $GB = 22.3499\ MHz$, with a phase margin of $\Phi_M = 92.06754°$. Besides the simulated gain is less than the expected value of $|A_V| = 30\ V/V$ defined in section 4.4.1, it is still an acceptable value.

5.4.2 Current-Source Inverter Voltage Response

The VTC of the current-source inverter is obtained by replacing the ac voltage source from circuit Figure 5.16 by a dc voltage source. A capacitive load of $CL = 1\ pF$ is applied while performing a voltage sweep from $-1.5\ V \leq V1 \leq 1.5\ V$. The obtained

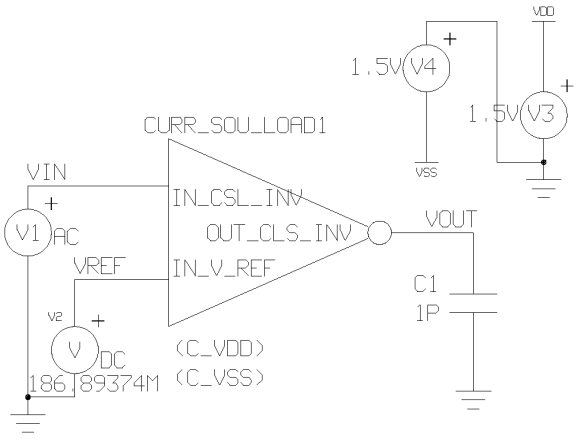

Figure 5.16: Circuit configuration for testing the frequency response of the current-source inverter.

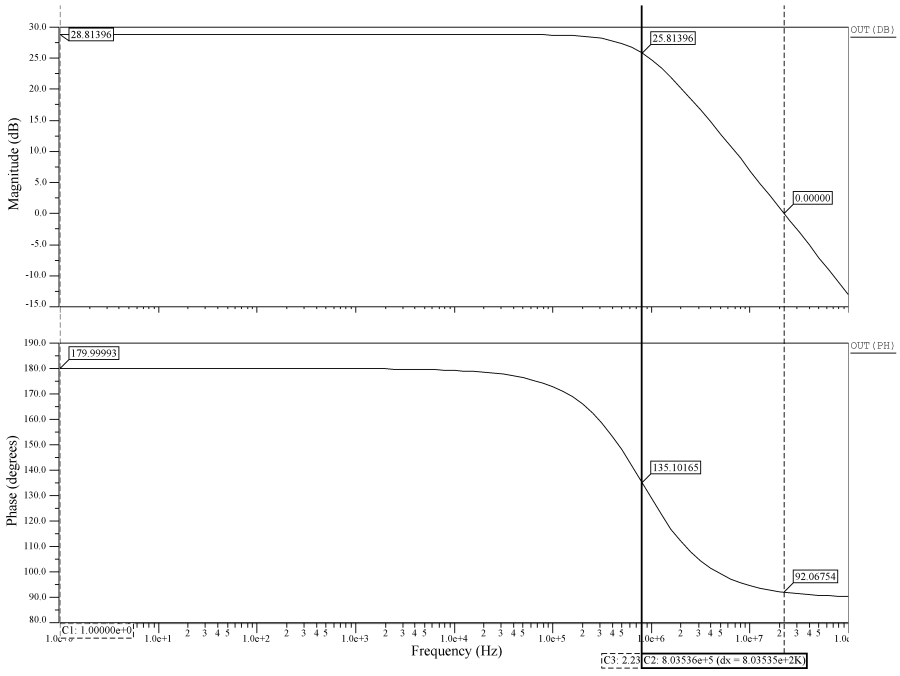

Figure 5.17: Frequency response from circuit of Figure 5.17.

VTC appears in Figure 5.18.

The Figure 5.18 illustrates an excellent linearity, with a threshold voltage $V_{th} = 11.05\ mV$. The saturation voltage limits are

$$-1.3\ V \leq V_{OUT} \leq 1.5V \tag{5.11}$$

The module presents an excellent performance, since $V_{th} \approx 0\ V$.

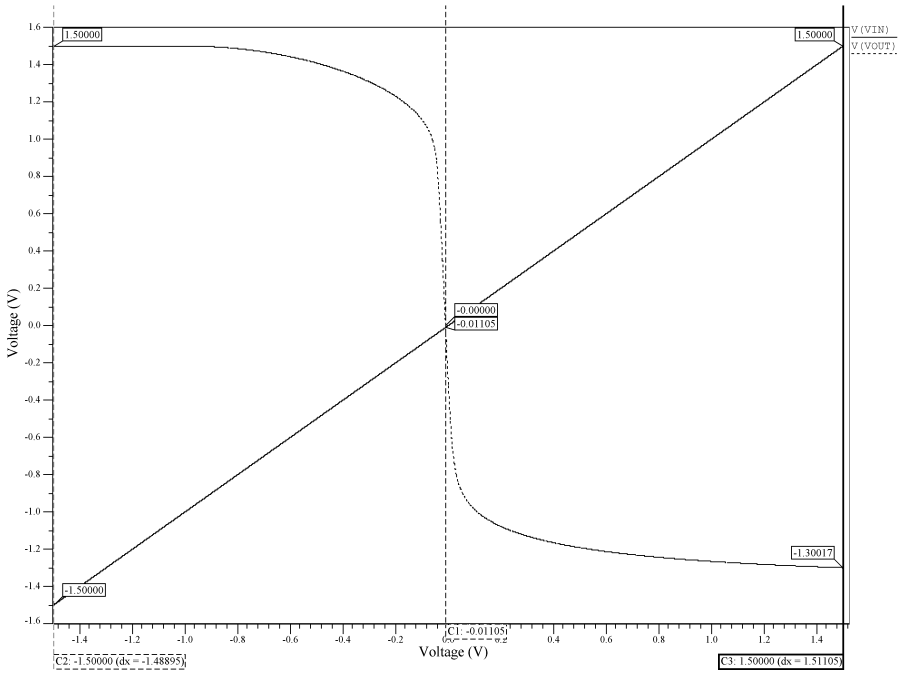

Figure 5.18: Voltage transfer curve from circuit of Figure 5.16.

5.4.3 Current-Source Inverter Time Response

The current-source inverter circuit appears in Figure 5.19. The circuit has a load of $CL = 1\ pF$, and the pulse waveform with a 10 μsec time delay. The plot from Figure 5.21 shows that the settling time for the falling edge is $t_{fall} = 66.15\ nsec$, while the settling time for the rising edge is $t_{rise} = 56.55\ nsec$, as shown in Figure 5.22 (note that the input pulse signal starts rising at time $t = 20.001\ \mu sec$ due to a 1 $nsec$ falling time delay).

The slew rate of the circuit can be found from Figure 5.22; with signal outputs at

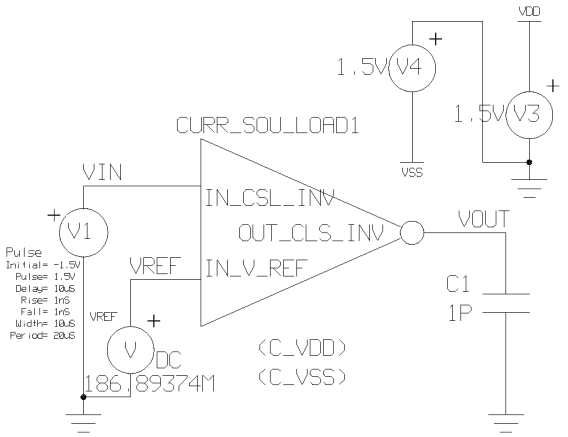

Figure 5.19: Circuit configuration for testing the time response of the current-source inverter.

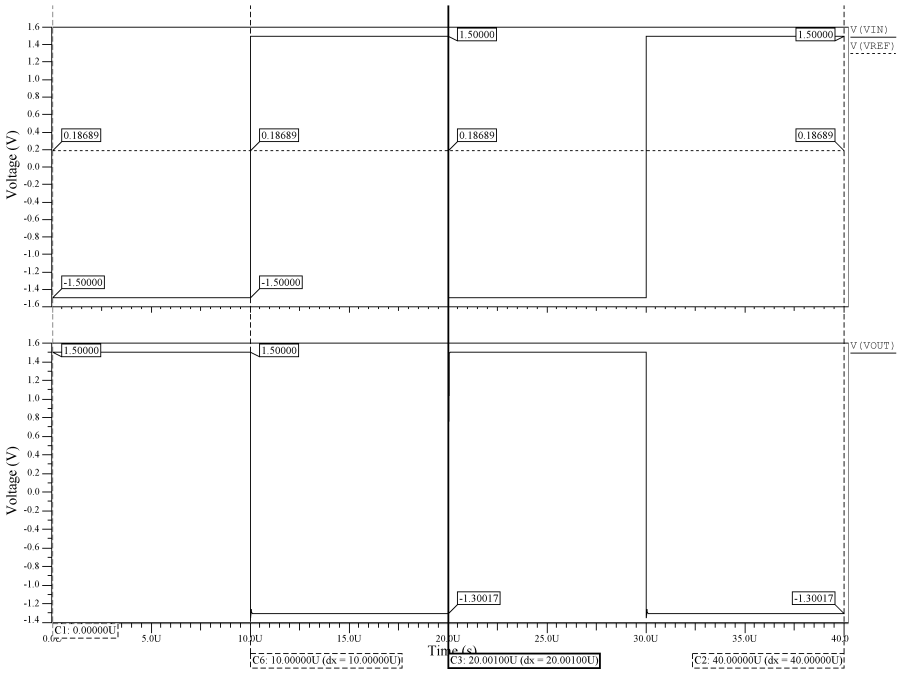

Figure 5.20: Current-source inverter time response.

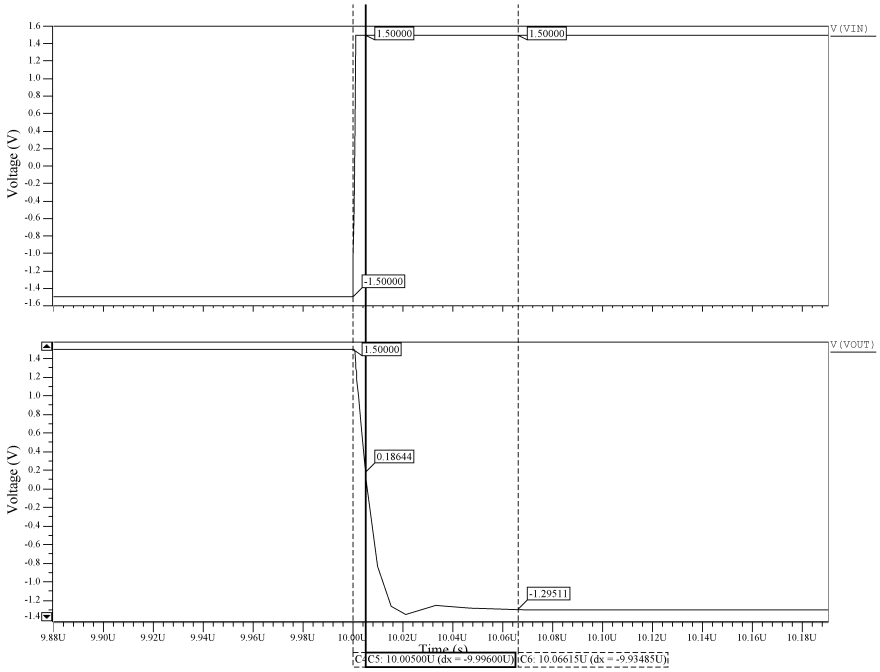

Figure 5.21: Closer view at the output falling edge of the current-source inverter waveform.

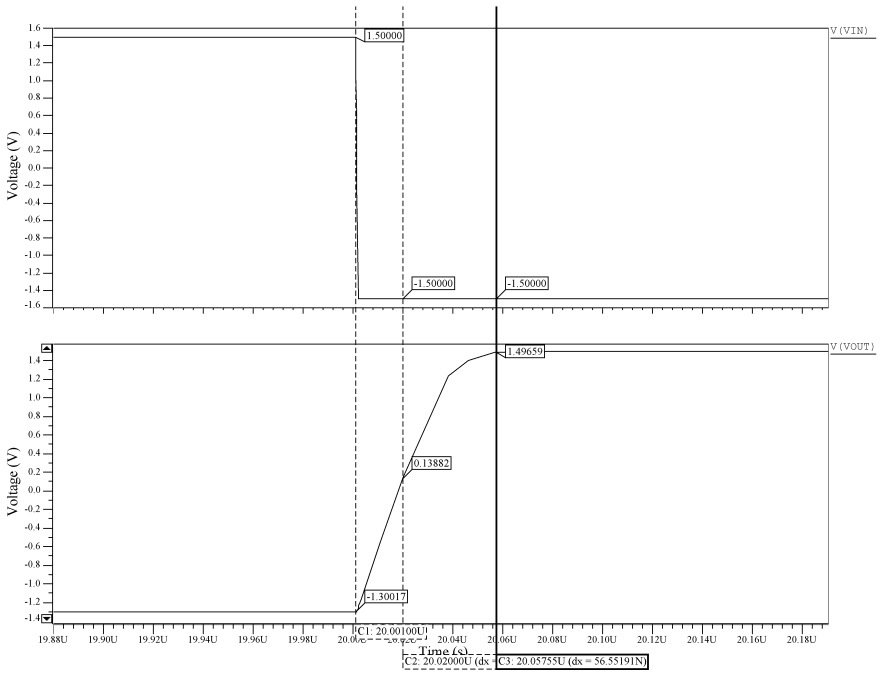

Figure 5.22: Closer view at the output rising edge the current-source inverter waveform.

$$t_1 = 20.001\ \mu sec$$
$$t_2 = 20.02\ \mu sec$$

Observing the output voltages at t_1 and t_2

$$V_{OUT1} = -1.30017\ V\ @\ t = t_1$$
$$V_{OUT2} = 0.13882\ V\ @\ t = t_2$$

The average slew rate, SR, according to Eq. (5.14) is

$$SR \approx 75.7363\ V/\mu sec \tag{5.12}$$

5.4.4 Triple Push-Pull Inverter Voltage Response

The Figure 5.23 shows the circuit used to obtain the VTCs from each of the inverter amplifiers that integrate the comparator inverter module (see Figure 4.36). A dc voltage source is connected to the input terminal and a capacitive load of $CL = 1PF$ to the output terminal. The obtained simulations are shown in: Figure 5.24, Figure 5.25, and Figure 5.26, respectively.

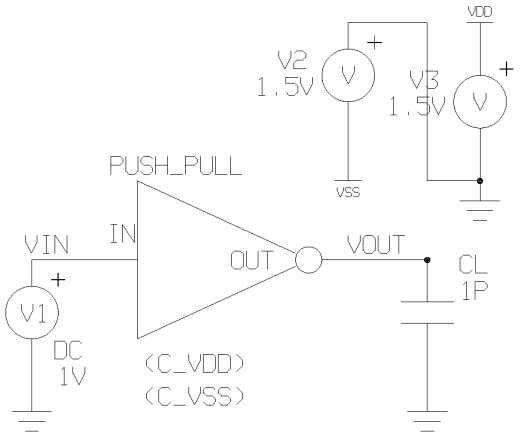

Figure 5.23: Circuit configuration for measuring the voltage transfer curve of each of the push-pull inverter amplifiers.

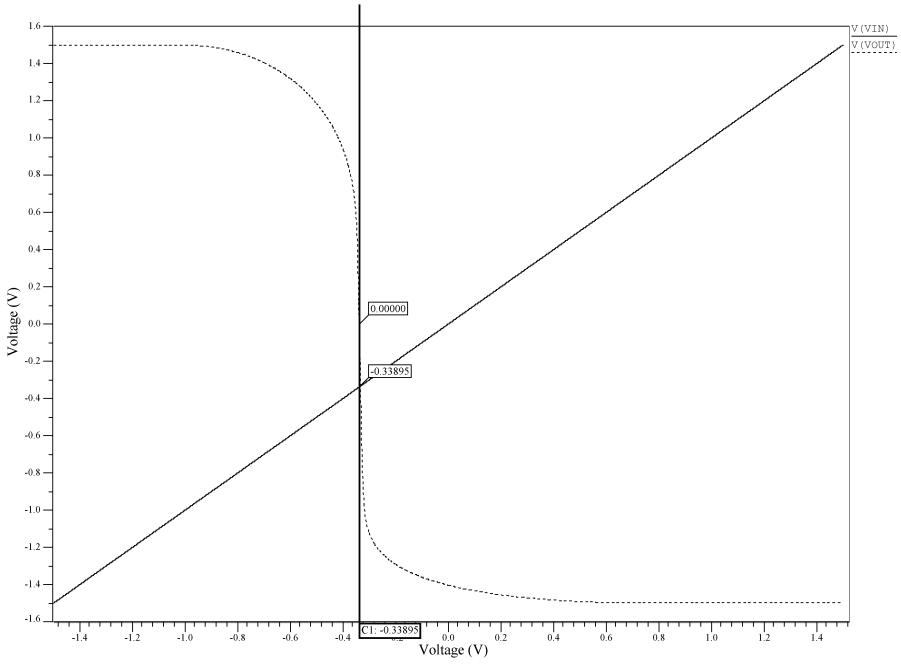

Figure 5.24: Voltage transfer curve of inverter A module.

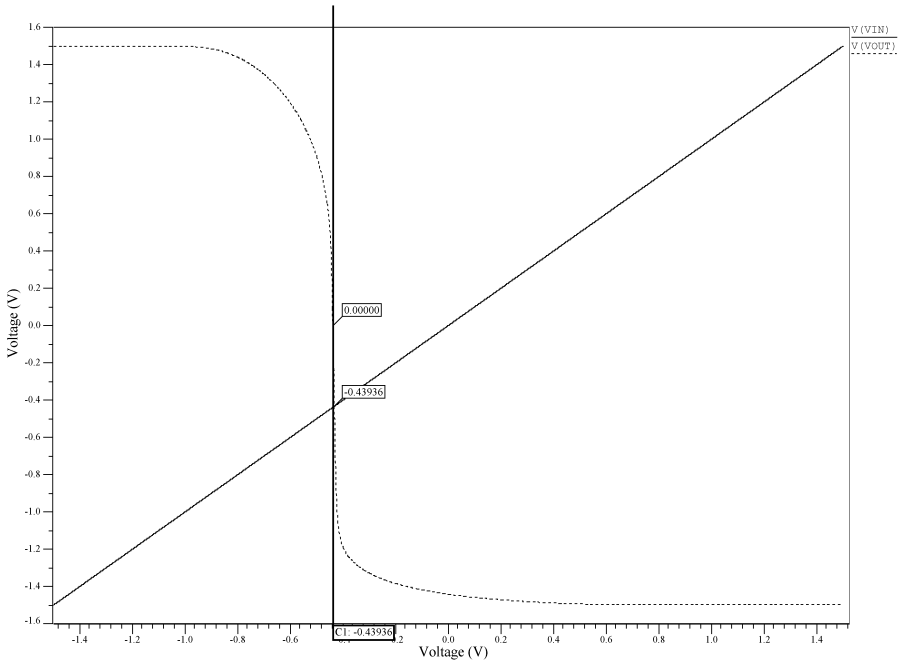

Figure 5.25: Voltage transfer curve of inverter B module.

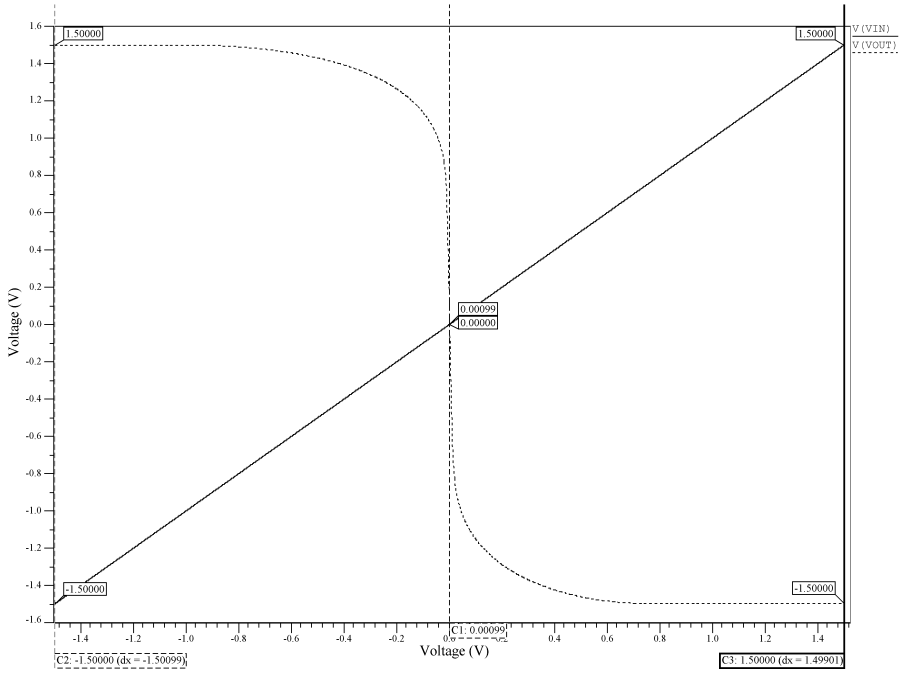

Figure 5.26: Voltage transfer curve of inverter C module.

The obtained threshold voltage for inverter A module is $V_{th}(A) = -338.95\ mV$, and the threshold voltages for inverter B module and inverter C module, are $V_{th}(B) = -439.36\ mV$ and $V_{th}(C) = 990\ \mu V$, respectively.

Once defined all individual inverter modules, they are integrated on the comparator inverter circuit module, shown in Figure 4.36. The VTC obtained from the circuit appears in Figure 5.27.

The threshold voltage of this triple push-pull inverter circuit, is $V_{th}(Comp) = -332.66\ mV$, and it compensates the offset voltage generated from previous stages. Therefore, this circuit is capable of increasing the amplitude of a signal up to 1.5 million times (taking the worst case of an input signal amplitude of $V_{IN} = 1\ \mu V_P$). This allows an output amplitude of 1.5 V_P by conditioning the original input signal to prepare the frequency for measurement.

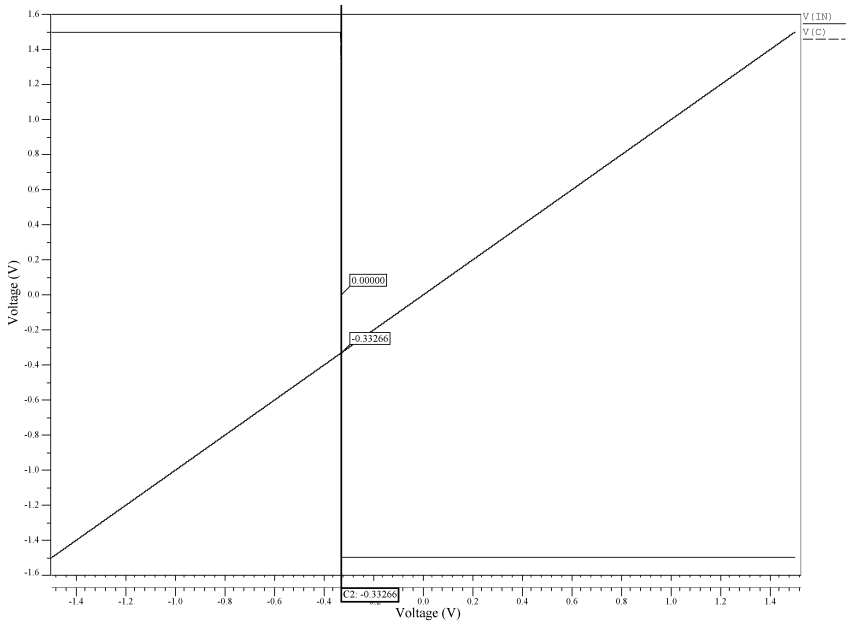

Figure 5.27: Voltage transfer curve of the triple push-pull inverter with a load of $CL = 1\ pF$.

5.5 Signal Conditioning System Simulation

This section describes the simulation analysis of the complete signal conditioning system. Frequency, voltage and time analysis are simulated and their results are explained in detail.

5.5.1 System Frequency Response

Figure 5.28 shows the circuit configuration for measuring gain and phase response for the complete signal conditioning system. An ac source, $V1$, is connected to the input terminals of the device, and a capacitive load of $CL = 10\ pF$ to the output terminal, OUT. Simulation results are shown in Figure 5.29.

From simulations, the signal conditioning system behaves as a comparator, therefore simulation shows a gain of $A_V = 148.4009\ dB$. However it is not relevant, since the complete system behaves as a comparator amplifier. The cut-off frequency is $f_{(-3dB)} = 78.7961\ kHz$. The operating frequency of the system is less or equal to $f_{IN}(max) = 50\ kHz$, though.

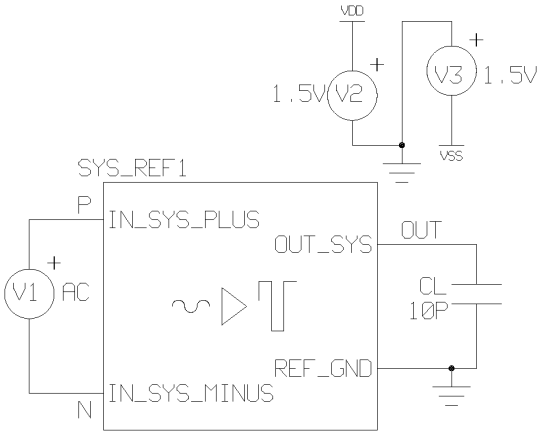

Figure 5.28: Circuit configuration for testing the open-loop frequency response of the complete system.

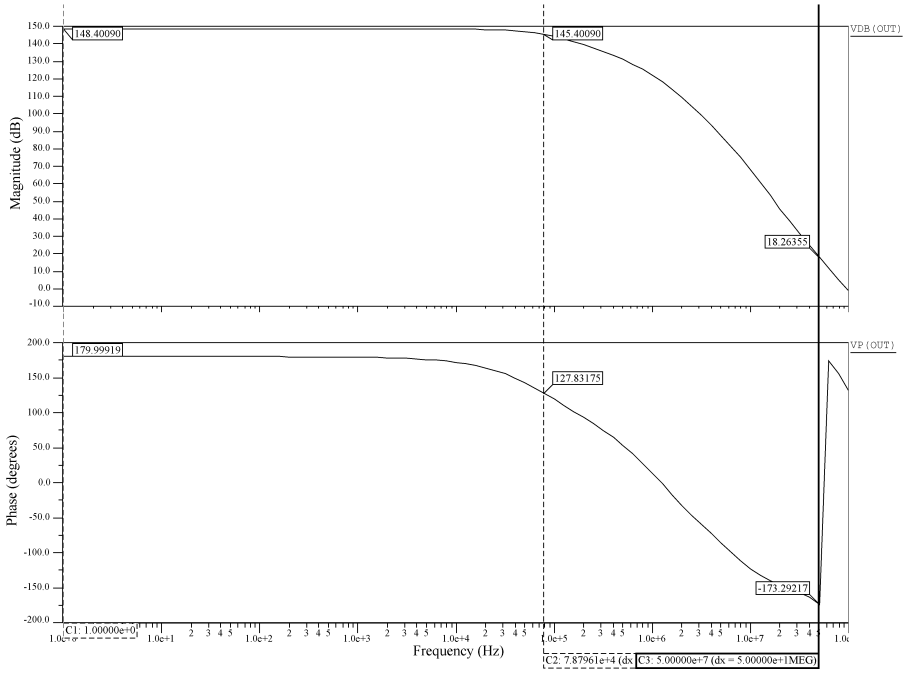

Figure 5.29: Frequency response from circuit of Figure 5.28.

5.5.2 System Voltage Response

Circuit linearity is measured by replacing the ac voltage source (at the input terminals) by a dc voltage source; then, a sweep of $-1.5\ V \leq V1 \leq 1.5\ V$ can be performed. The obtained VTC is shown in Figure 5.30. A very good linearity can be observed, and the measured offset voltage is $V_{OS} \approx -40\ \mu V$. Moreover, saturation voltage is given as

$$V_{SS} \leq V_{OUT} \leq V_{DD} \tag{5.13}$$

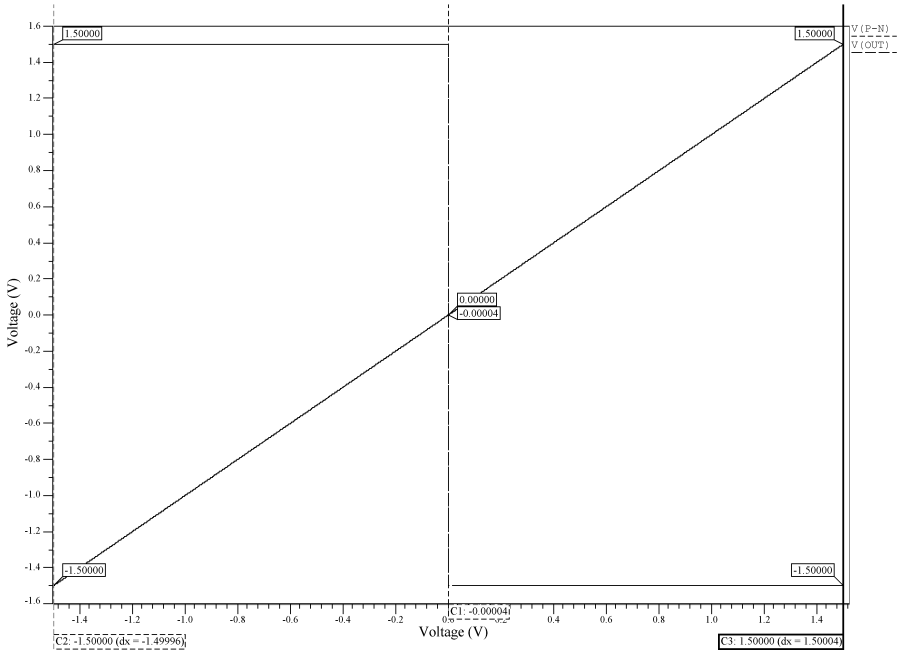

Figure 5.30: Voltage transfer curve from circuit Figure 5.28.

5.5.3 System Time Response

A pulse waveform with amplitude of $V_{PULSE} = 0.8\ V$, a period of $T = 20\ \mu sec$ and a duty cycle of $DT = 50\ \%$ feeds the overall system as shown in Figure 5.31. The circuit has a load of $CL = 10\ pF$, and the pulse wave has a 10 μsec delay. The plot from Figure 5.32 shows that the settling time for the output signal rising edge is $t_{rise} = 789.05\ nsec$, while the settling time for the falling edge is $t_{fall} = 608.58\ nsec$. The settling times for the complete system are fast enough to handle input signal frequencies up to $f_{IN} = 50\ kHz$.

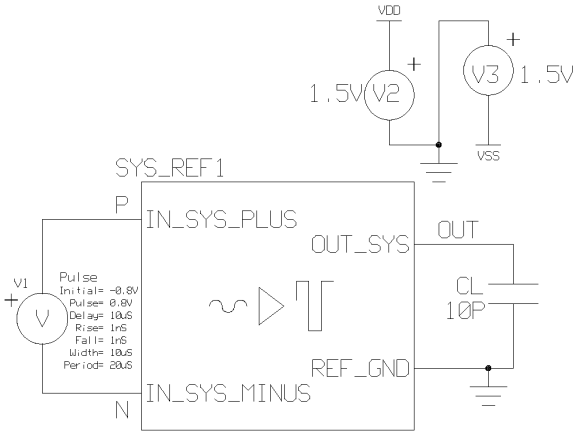

Figure 5.31: Circuit configuration for the testing time response of the signal conditioning system.

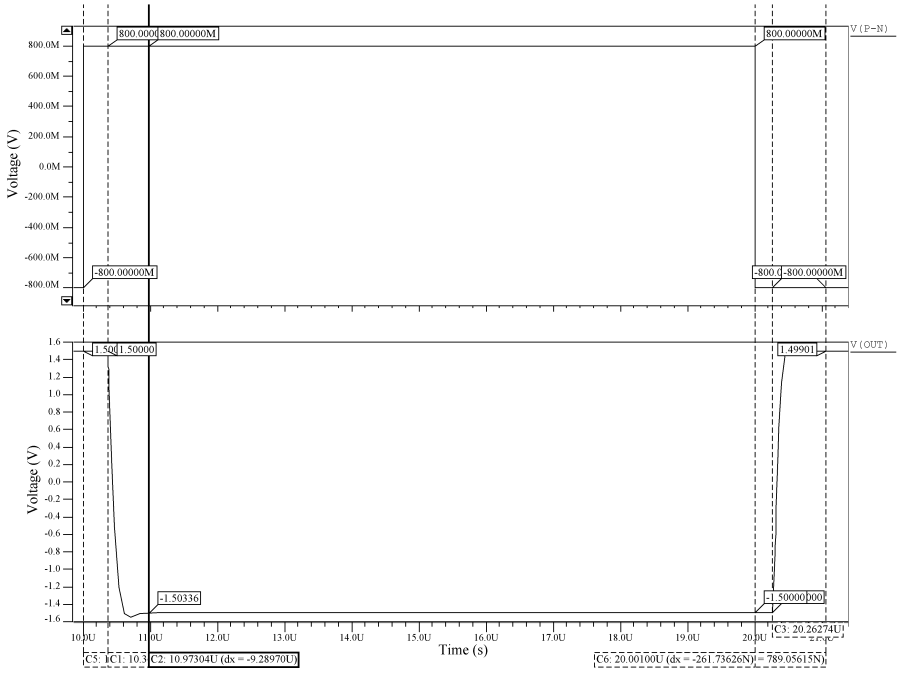

Figure 5.32: Time response from circuit of Figure 5.31.

In order to verify the resolution of the system, the plot from Figure 5.33 details the simulation of an input voltage source of $V_{PULSE} = 1\ \mu V$ applied to the system circuit from Figure 5.31. The graph shows that the settling time for the output signal rising edge is $t_{rise} = 1.20773\ \mu sec$, while the settling time for the falling edge is $t_{fall} = 864.87\ nsec$.

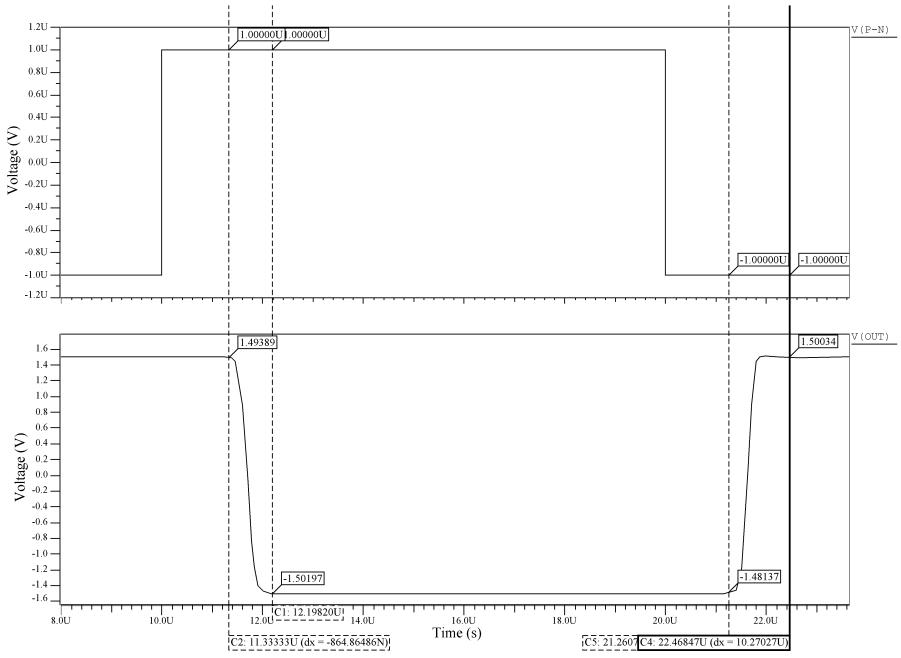

Figure 5.33: Time response from circuit of Figure 5.31 with an applied input of $V_{PULSE} = 1\ \mu V$.

The positive transition slew rate is calculated from Figure 5.34 and by using Eq. (5.14) as follows

$$\begin{aligned} V_{OUT1} &= -1.16432\ V\ @\ t_1 = 21.52\ \mu sec \\ V_{OUT2} &= -0.11190\ V\ @\ t_2 = 21.62\ \mu sec \end{aligned}$$

The average slew rate, SR, is given as

$$SR = \frac{-0.1119\ V - (-1.16432\ V)}{21.62\ \mu sec - 21.52\ \mu sec}$$

$$SR = 10.5242\ V/\mu sec$$

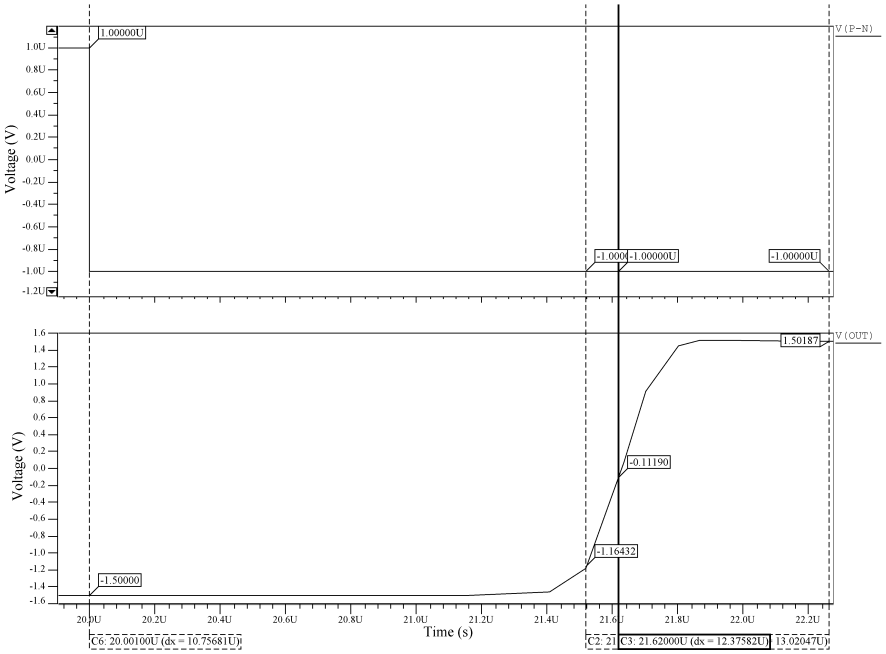

Figure 5.34: Closer view at the output rising edge of Figure 5.33.

As a comparison of the system circuit performance, Figures 5.35 and 5.36 show the transient response generated by an input $V_{IN} = 1\ \mu V$ at 10 kHz and 100 kHz respectively. Note that in both cases, the output signal is a $\pm 1.5\ V$ squarewave signal. Although the output signal phase differs on the input signal phase, the frequency of the input signal is maintained along the signal conditioning circuit.

When input frequency increases, the system is not able to operate properly. Therefore, the output signal is not a squarewave signal anymore. As an example, Figure 5.37 shows the system output response for an input of $V_{IN} = 1\ \mu V$ at 500 kHz.

5.5.4 Discussion of Simulation Results

Simulations of the integrated system show some limitations. The maximum operating frequency, delimited by $f_{(-3dB)}$, is about 50 kHz. Therefore, the frequency response capability of the system covers the the operating range of typical MEMS resonant sensors [7, 41]. Moreover, the final offset voltage measured is even less than the OTA offset voltage, due to the compensation of the inverter amplifier stages by controlling their threshold voltage, V_{th}, as expected [31]. Another important benefit from the inverter amplifier stages is the fast SR of the system, about 10 $V/\mu Sec$, considering

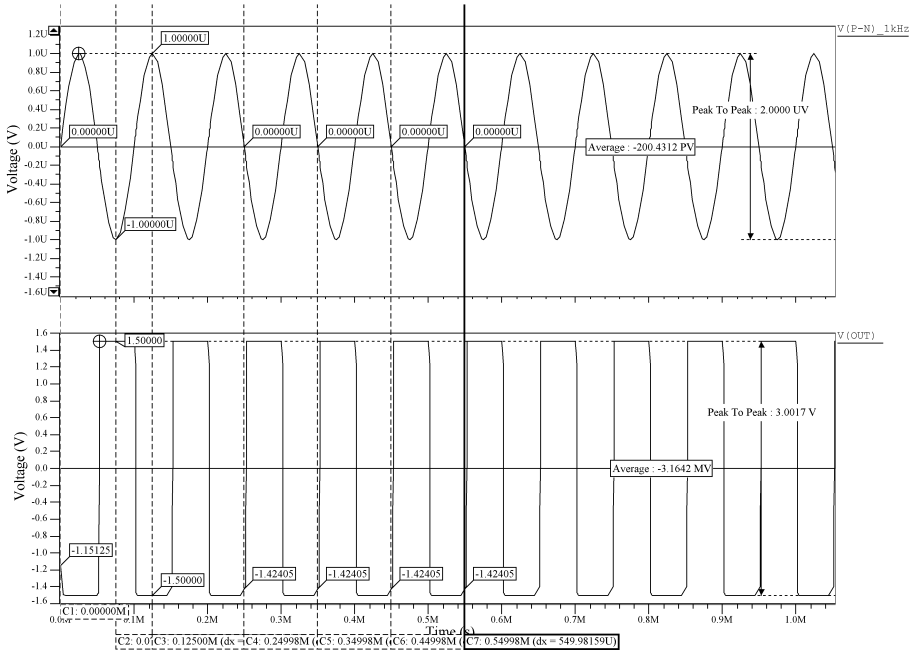

Figure 5.35: Transient response from circuit of Figure 5.31 with an applied input of $V_{IN} = 1\ \mu V$ at 10 kHz.

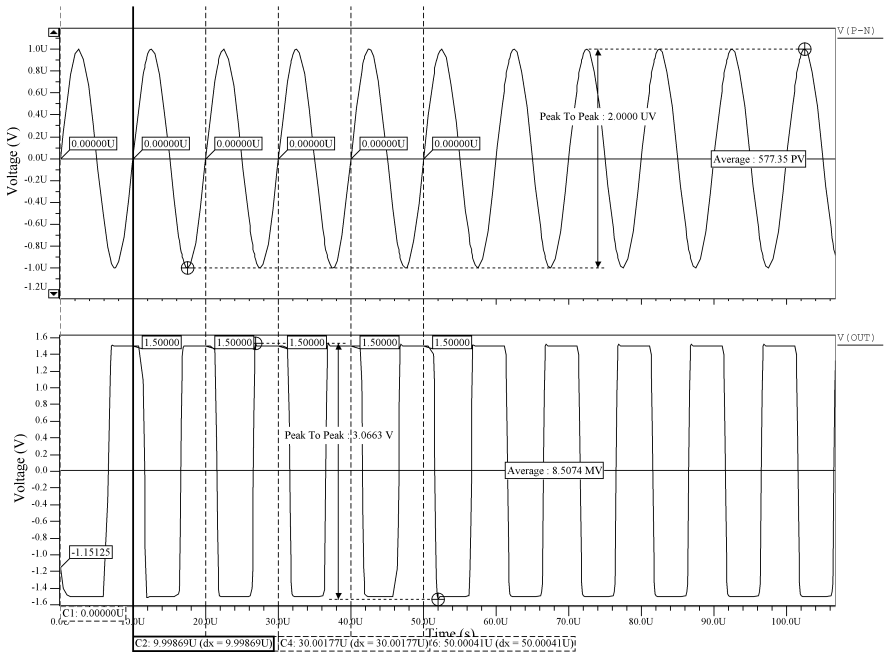

Figure 5.36: Transient response from circuit of Figure 5.31 with an applied input of $V_{IN} = 1\ \mu V$ at 100 kHz.

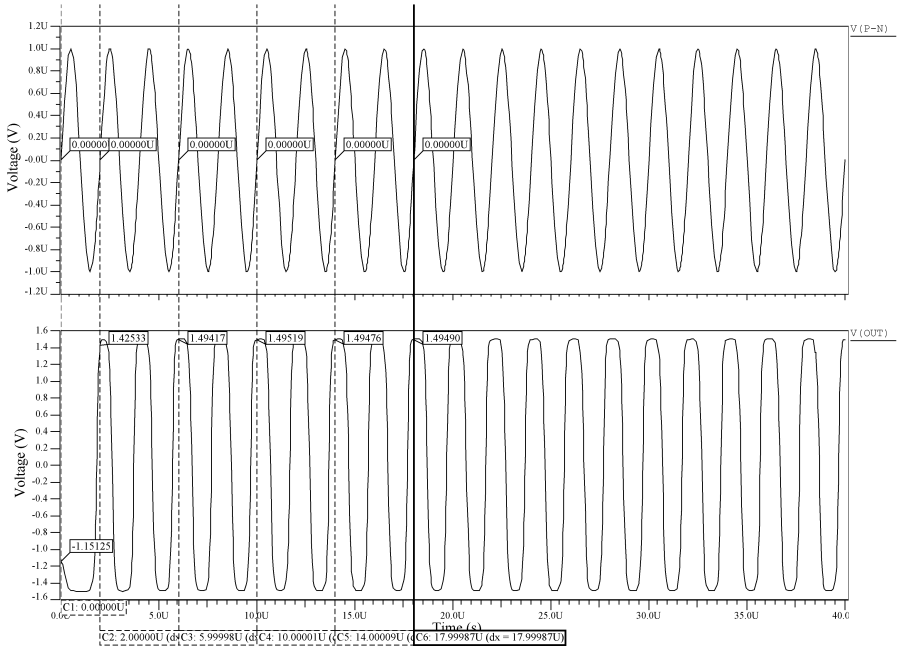

Figure 5.37: Transient response from circuit of Figure 5.31 with an applied input of $V_{IN} = 1\ \mu V$ at 500 kHz.

that the design consists on an analog interface circuit with 74 CMOS transistors, 3 polysilicon capacitances and a single polysilicon resistance.

The phase margin of $\Phi_M = 71.3157°$ obtained from the OTA frequency simulation, confirm the stability of the basic module of the complete system. Moreover, from transient analysis, the slew rate was obtained. During falling edge, the signal performs faster than during rising edge, thus, only the rising edge is assumed as critical for slew rate measurement.

Finally, even the frequency simulation indicates that the maximum operating frequency of the system is $f_{(-3dB)} = 78.7961\ kHz$, the transient response simulations show that the system behaves properly at $f_{IN} = 100\ kHz$. There is a phase shift, however, which increases when the input frequency rises. Nevertheless, the final frequency signal is the same that the original, no matter the phase shift. If the input signal frequency is higher than 100 kHz, the output signal can not achieve the squarewave form. Therefore, simulations showed that the system is not able to operate with frequency signals higher than $f_{IN} \approx 100\ kHz$, since the output signals will not have a squarewave form.

Chapter 6

Layout Design

6.1 Introduction

This chapter describes the layout implementation of the signal conditioning circuit designed in compliance to the CMOS AMS® 0.35 μm technology process parameters. The chapter presents, step-by-step, the physical design of the individual circuit modules, the integration of the modules through the layout design flow, and the complete layout of the schematic circuit diagram shown in Figure 4.38. The first modules illustrated in this chapter are the inverter amplifier circuits. Although they are not part of the first circuit stage, inverter amplifiers are easier to translate from schematic to layout than the differential pair schematic circuit. The following module is the OTA, for which the layout is more complicated than an inverter layout. After the OTA, the layout implementation of the instrumentation amplifier is shown in detail. Finally, the integration of the signal conditioning layout is developed.

To have a clear and practical description of the layouts designed for each module, some layers required for fabrication are hidden, and an ideal layout is shown. However, if the component placement and the circuit routing are well characterized, more layers will not appear in the Figures. These hidden layers are included in the design files and they could be visible by changing their properties from ICstudio® layout tool [49]. A detailed explanation of the technical aspects of designing with ICstudio® and a complete methodology can be found in [50].

The visible layers of the following layouts are illustrated in Figure 6.1. The drawing scale is micrometers (μm).

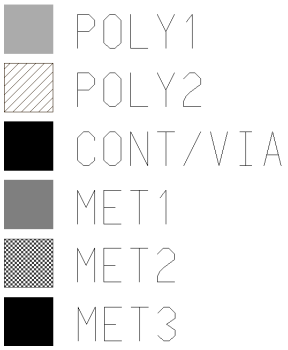

Figure 6.1: Layer stack for layout.

6.2 Inverter Push-Pull Inverter

The individual layouts of push-pull inverter modules A, B, and C (based on both, transistor sizes from Table 4.12, and schematic Figure 4.31, are shown in Figures 6.2, 6.3, 6.4, respectively.

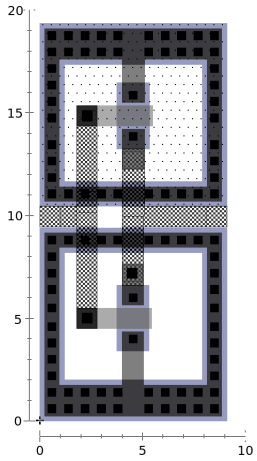

Figure 6.2: Layout of the push-pull inverter module A.

As in the schematic circuit diagram, the lower device corresponds to the n-channel transistor, $M1$, and the upper device corresponds to the p-channel transistor, $M2$. Although all transistors differ on their size, in order to keep a symmetric layout, a standard height of 19.35 μm is defined for those three modules. The surrounding frames of both devices, correspond to the bulk connected to *metal1* layer. Note that they are two separated frames

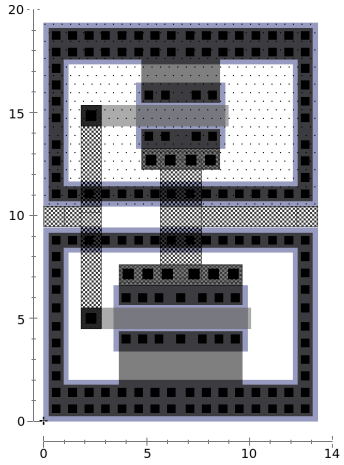

Figure 6.3: Layout of the push-pull inverter module B.

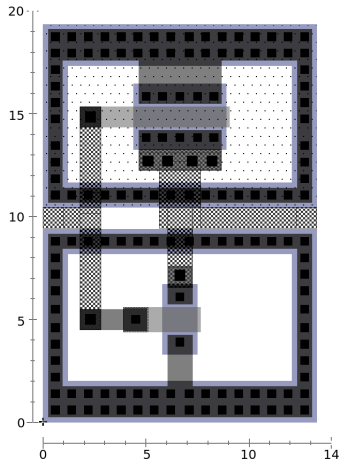

Figure 6.4: Layout of the push-pull inverter module C.

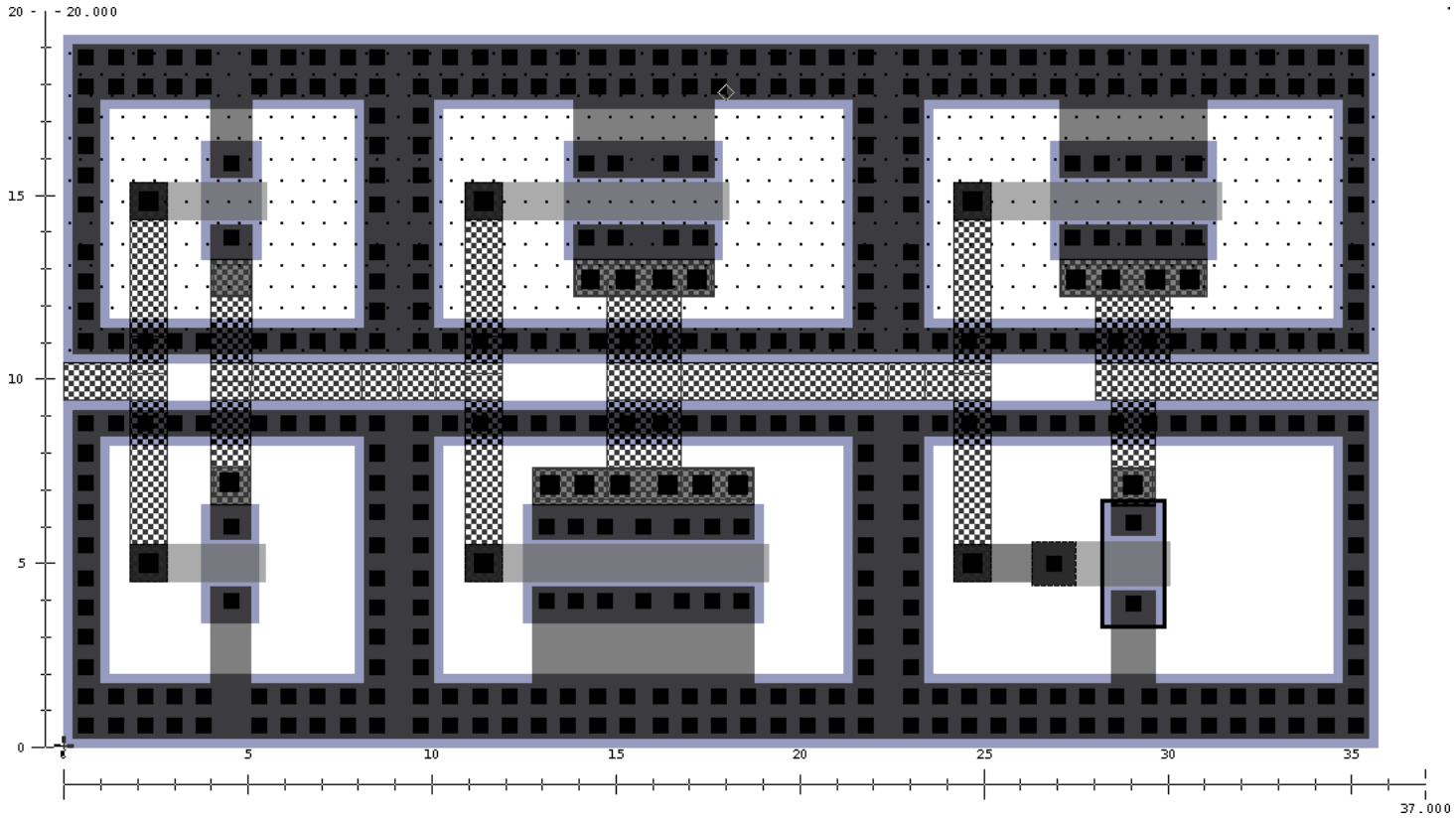

Figure 6.5: Layout of the triple inverter module .

a) One frame connected to the p-substrate (n-channel bulk)

b) One frame connected to the n-well substrate (p-channel bulk). By configuring the push-pull inverter amplifiers as the triple inverter amplifier from Figure 4.36, the layout shown in Figure 6.5 is obtained.

From Figure 6.5, we can observe several features presented in the layout: all transistors are oriented the same way, and none of them is folded[1]. Moreover, since the substrate tie connections are all over *metal1* layer, the signal ports are routed over *metal2* layer through the different modules. The width of the metal layers routing are big enough to handle large amounts of current (according to current density values $[mA/\square]$ specified in AMS® confidential documentation). Another relevant characteristic, is that the signal routing over any device is avoided.

6.3 Current-Source Inverter Amplifier

The layout of the current-source inverter amplifier (based on both, transistor sizes from Table 4.11, and schematic Figure 4.28, is shown in Figure 6.6, where the lower device corresponds to the n-channel transistor, $M1$, and the upper device corresponds to the p-channel transistor, $M2$. As seen in Figure, $M2$ device is folded into two transistors sharing a common *drain*, which is connected to the output terminal and to the *drain* of $M1$ device as well. This connection is over *metal2* layer.

The two gates of $M2$ are connected with *metal1* layer, the input terminal is on *metal2* layer, though. Therefore, the *metal1* connection of gates from $M2$, changes to *metal2* layer for connecting it to the input terminal. The same case occurs for $M1$ device.

6.4 Operational Transconductance Amplifier

This section discusses, first, the layout of the differential pair circuit and the load inverter circuit. Next, the bias voltage circuit and the bias current circuit layout design are explained. Finally, the integration of all layouts into a single OTA layout module is shown.

[1] *Folding* a MOS transistor consists of split it into smaller width subtransistors, sharing common drains and/or sources [see Figure (2.19)].

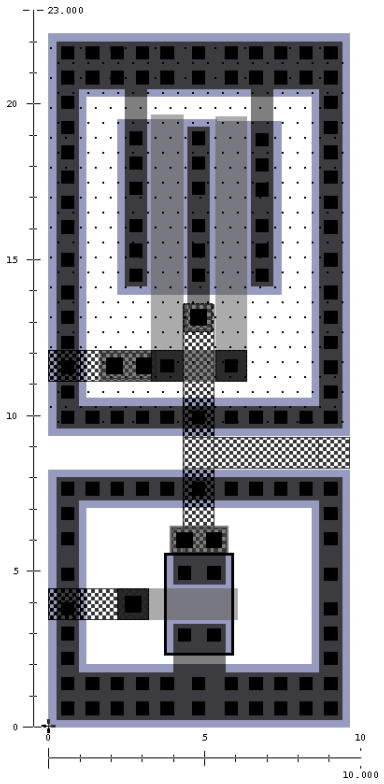

Figure 6.6: Layout of the current-source inverter module .

6.4.1 Differential Pair Circuit

The layout of the differential pair amplifier (based on both, transistor sizes from Table 4.8, and schematic circuit of Figure 4.12), is shown in Figure 6.7.

On this design, input devices consist on four transistors cross-connected in order to improve matching; this layout technique is called *cross-quading* and allows better electrical and thermal matching. Figure 6.8 shows a closer view of the four input transistors placement [23]. The input transistor $M1$ is placed on the opposite corner of transistor $M1\_B$. For devices $M2$ and $M2\_B$ the same placement is applied. Note that input signals paths are located horizontally in the middle of the four input devices with four *metal1* layer paths, and since the same node is in opposite corners, the input paths are crossed, just in the middle of the circuit, making only two circuit nodes from those four paths. When the crossing-connection is made, one path is wired over *metal2* and the other is wired over *metal3*.

6.4.2 Current-Source Load Circuit

The layout of the current-source load (based on both, transistor sizes from Tables 4.6, 4.5, and schematic circuit of Figure 4.14), is shown in Figure 6.9. The layout dimension is 80 $\mu m\times$ 60 μm.

The total area of the compensation capacitance is notable, compared to the compensation transresistance, $M8$, located on the left side of the capacitance. Also, on the right side of the capacitance, transistors $M6$ and $M7$ are located, downside and upside each other, respectively. All devices routing is made on *metal2* layer.

6.4.3 Bias Voltage Circuit

The layout of the bias voltage circuit module (based on both, transistor sizes from Table 4.6, and schematic Figure 4.16), is shown in Figure 6.10. The defined transistor sizes for this module do not permit a well symmetric layout design, as in the bias current circuit, but a vertical approach was defined: MOS transistors are stacked through the y axis. Moreover, in order to get photolitographic invariance, all devices are oriented vertically (their gates are parallel to the y axis).

A frame made of *metal1* layer surrounds $M4$ and $M1$ devices, and it is tied to the n-well substrate. This frame is connected to the most positive supply voltage. The

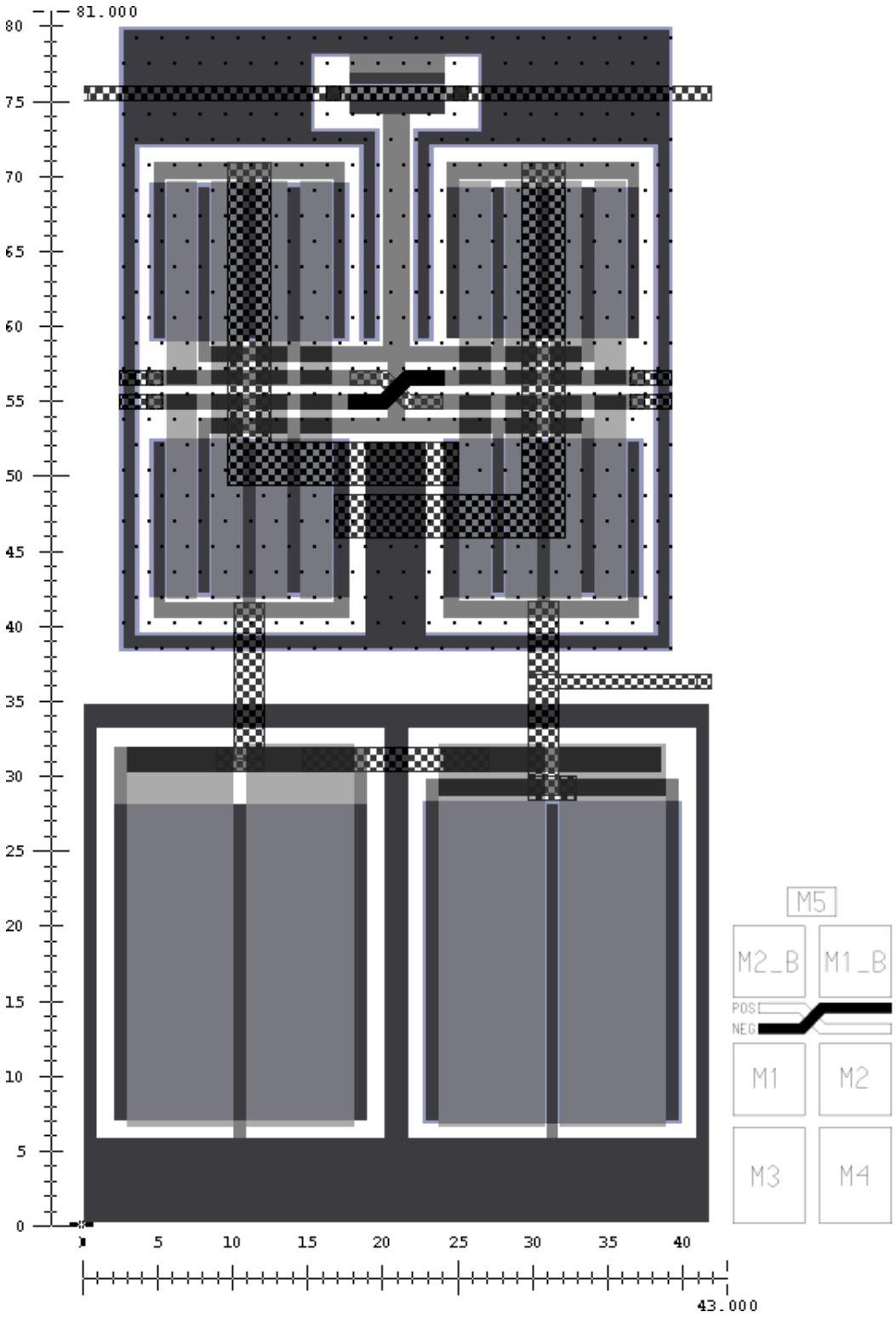

Figure 6.7: Layout of the differential pair amplifier module.

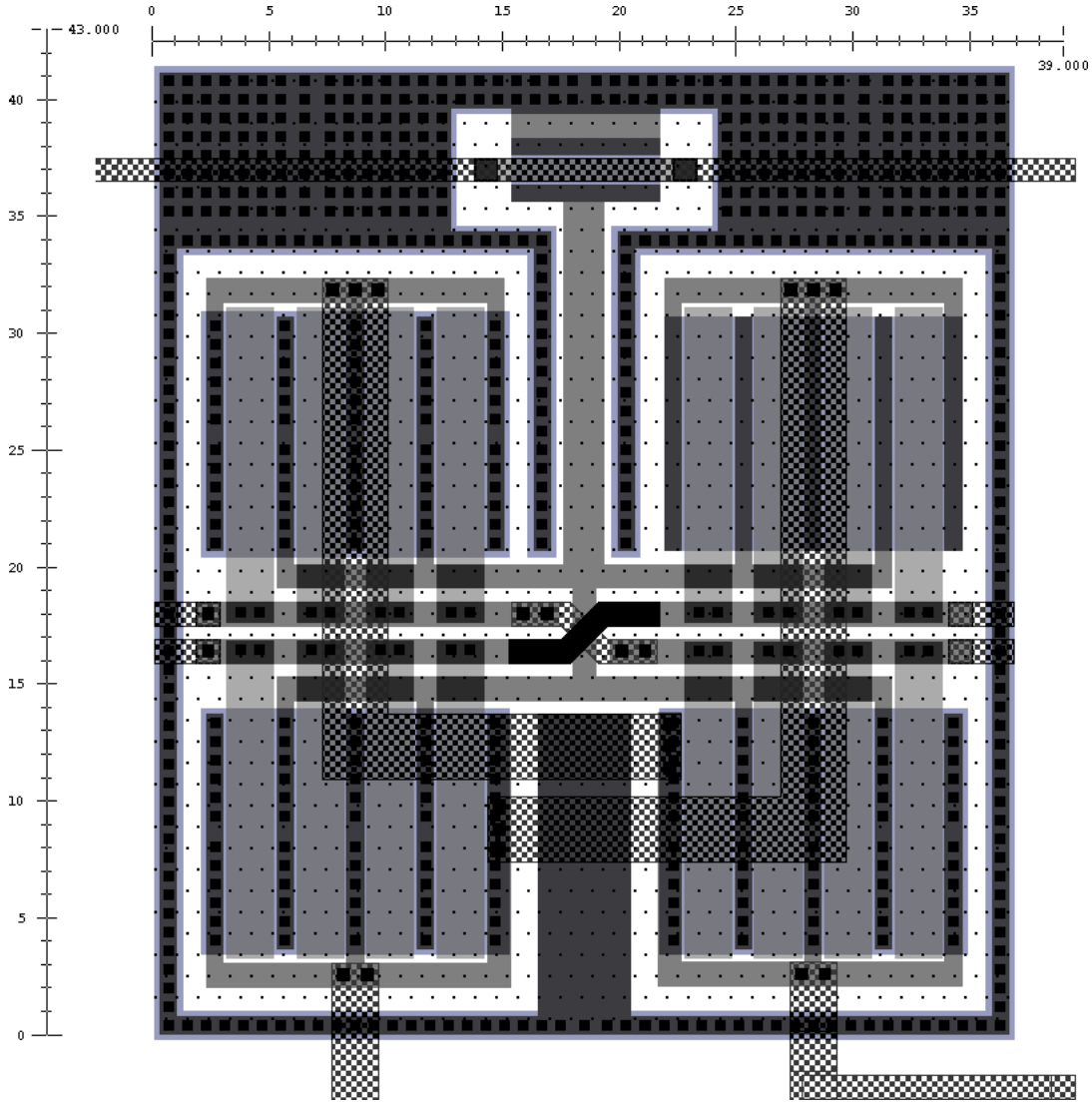

Figure 6.8: Detailed view of the input transistors of Figure 6.7.

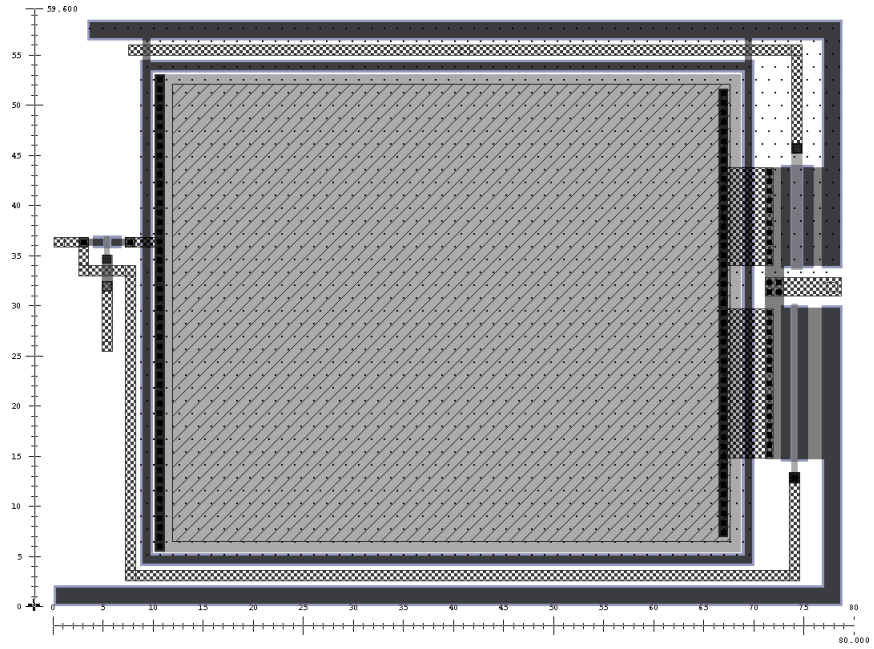

Figure 6.9: Layout of the current-source load module.

same design is for n-channel devices, where a frame made of *metal1* layer surrounds $M2$ and $M3$, and it is tied to the p-substrate. This frame is connected to the most negative supply. The connection between transistors $M1$ and $M2$ is routed in *metal3*. As in the other modules, the signal outputs are routed in *metal2* layer.

6.4.4 Bias Current Circuit

The layout of the bias current circuit module (based on both, transistor sizes from Table 4.7, and schematic Figure 4.18), is shown in Figure 6.11.

The common transistors size of this module (50 $\mu m \times 0.5$ μm), allows layout symmetry. Moreover, transistors $MC1$ and $MC2$ (which form the current mirror on top of the circuit) are *interdigitated* for improving their matching. The interdigitation technique was made by folding $MC1$ and $MC2$ into 4 subtransistors each other. The next step is to place the first two $MC1$ subtransistors on the left side of the folded device $MC2$, and the other two $MC1$ subtransistors on the right side of the folded device $MC2$ (as in Figure (2.18). The final step consisted on sharing drains and sources of both devices. The routing to $MC1$ and $MC2$ is over *metal2* layer, as well as the routing to $MC5$.

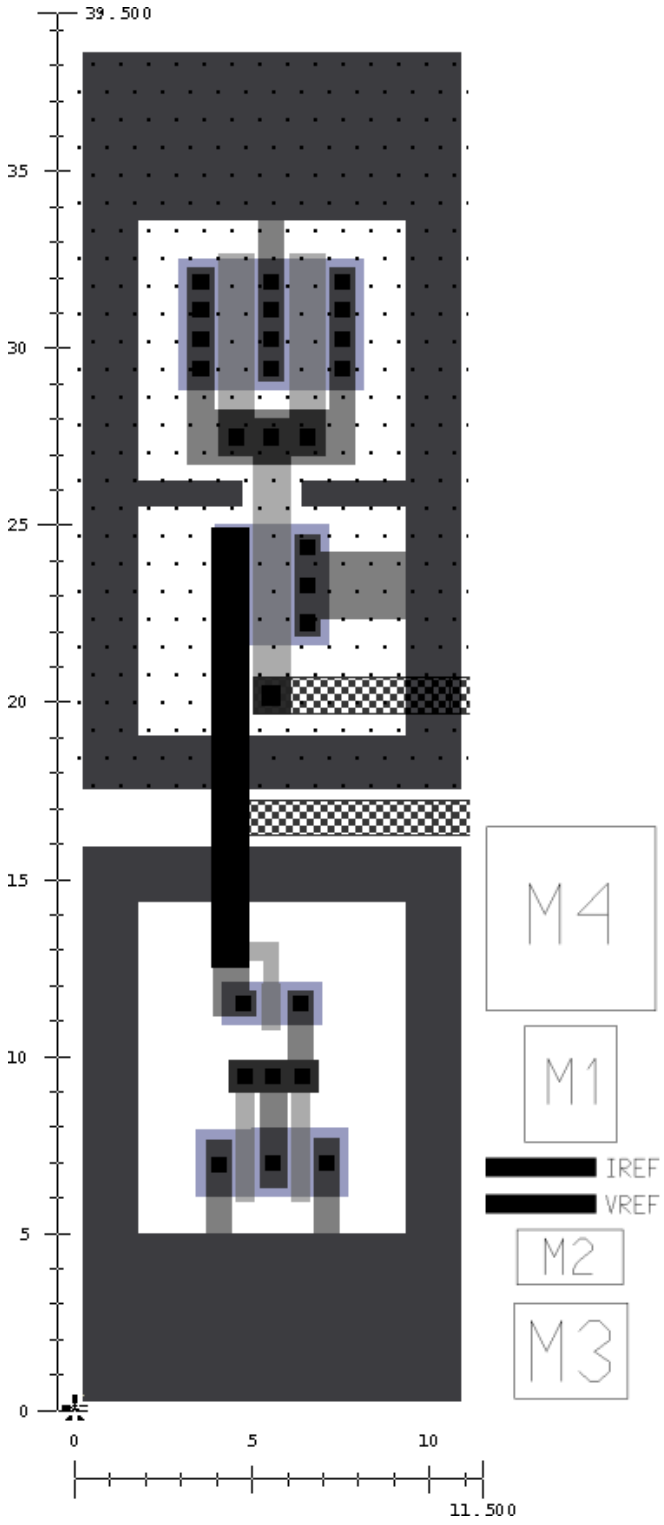

Figure 6.10: Layout of the bias voltage circuit module.

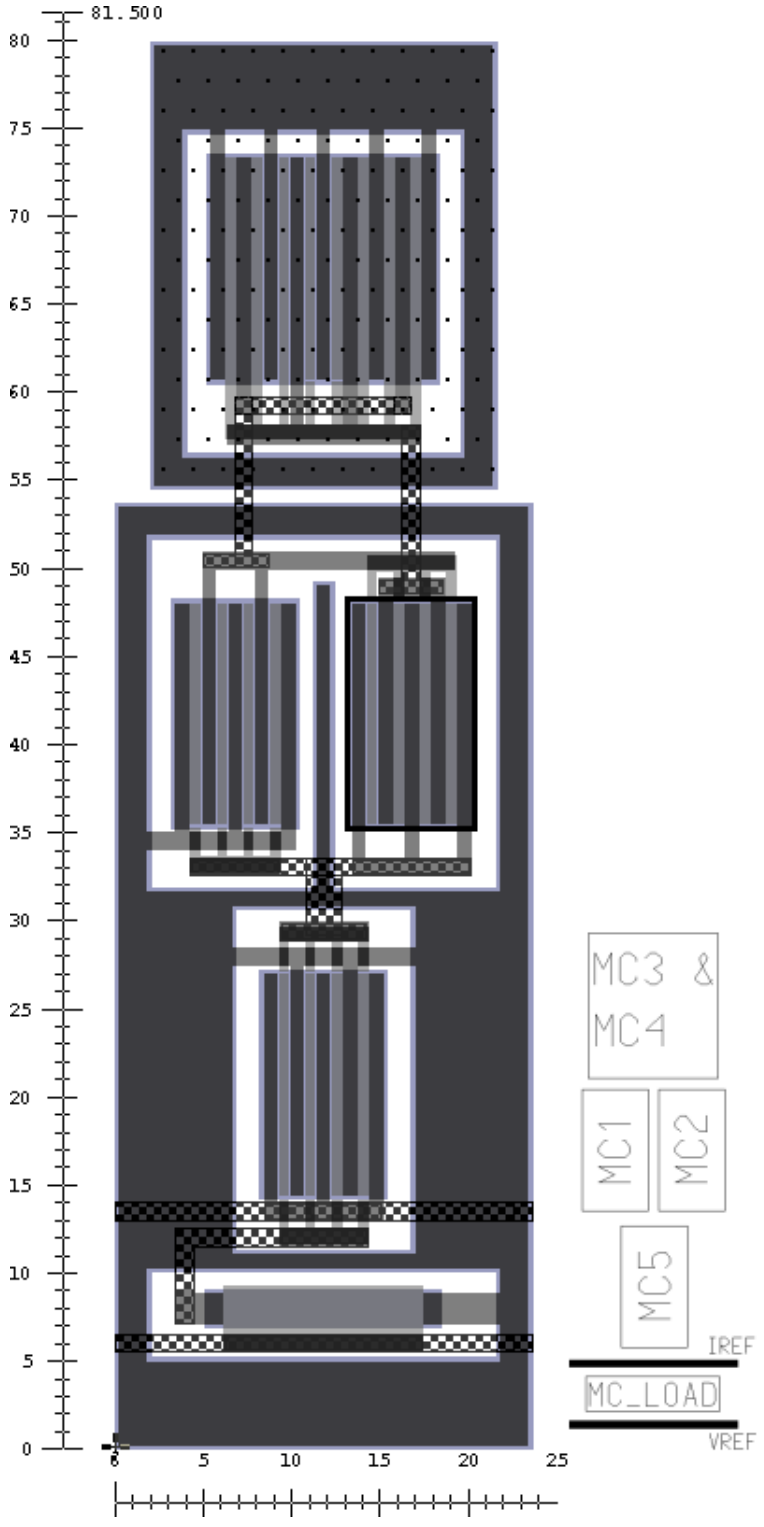

Figure 6.11: Layout of the bias current circuit module.

Orientation of bottom transistor, MC_LOAD, differs from the rest since its width and length sizes differ from the rest. The free surface of the circuit was filled with the *metal1* frames that serves as bulk connection for both, n-well and p-substrate.

6.4.5 OTA Layout

The Figure 6.12 shows the integration of all the functional modules of the OTA device. As mentioned earlier (Figure 4.20) the modular methodology also applies to the layout design.

The Figure 6.12 shows, from left to right the following modules: bias voltage, bias current, differential pair, and current-source load. Moreover, Figure 4.20 included an external connection for $VREF$, routed over *metal2* layer. The modified OTA layout that includes the $VREF$ output terminal appears in Figure 6.13. Note that the layout of internal modules is hidden and a rule indicates the extension of the $VREF$ bus towards the output terminal.

6.5 Instrumentation Amplifier

This section presents the layout of the instrumentation amplifier, explaining the placement of its components and their routing.

6.5.1 IA Complete Layout Design

Figure 6.14 shows the integration of the required circuit modules and transistors to develop the physical design of the IA.

Figure 6.14 shows $OPAMP\_A$ at the top of the layout, $OPAMP\_B$ at the bottom of the layout (and mirrored with respect to $OPAMP\_A$), and $OPAMP\_C$ in the middle of the previous two amplifiers, and horizontally flipped. Also included, polysilicon resistance, $R_G = 5\ k\Omega$, which is placed at the left of $OPAMP\_C$, just in the edge of the layout area.

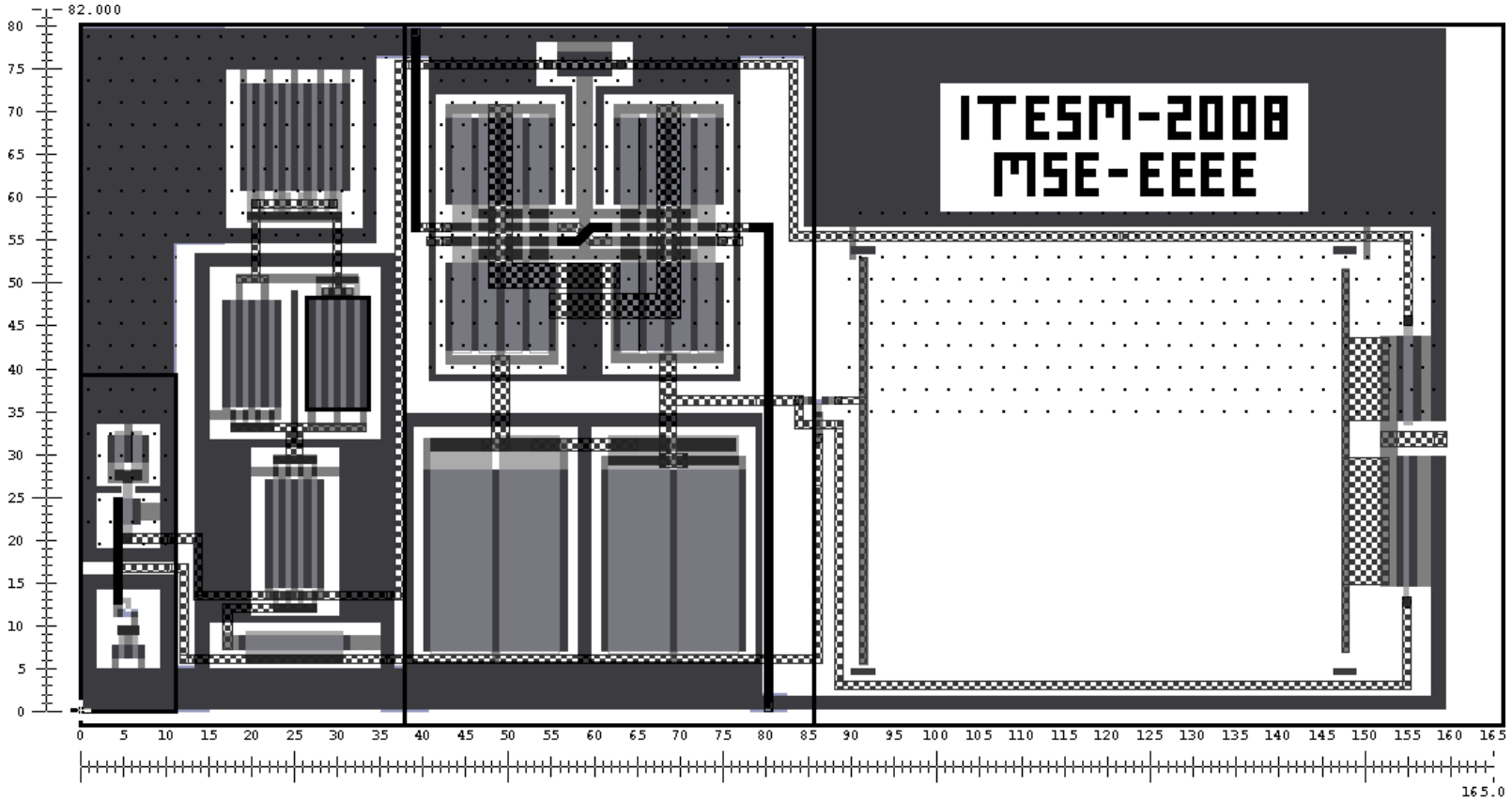

Figure 6.12: Layout of the OTA circuit module.

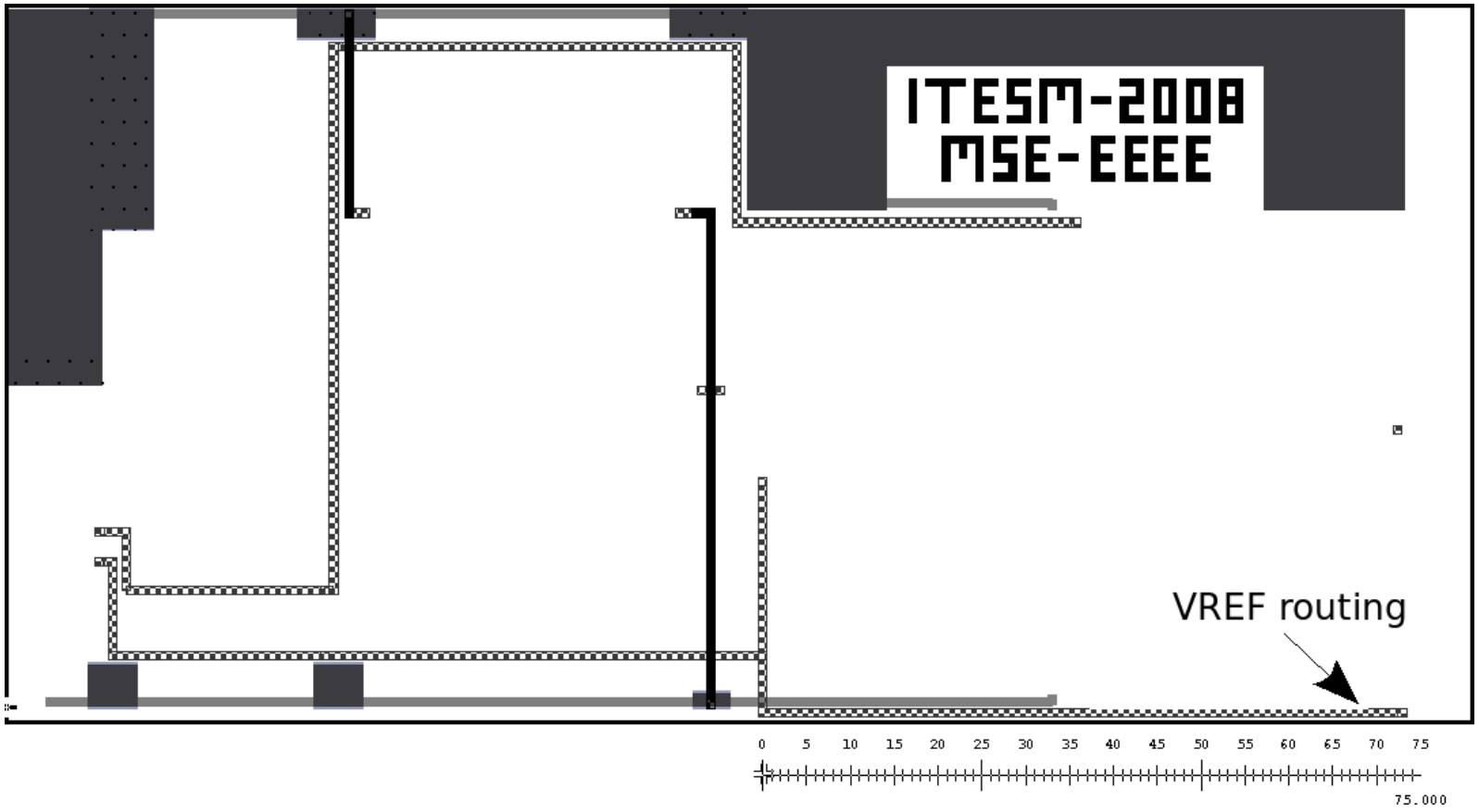

Figure 6.13: Layout of the OTA circuit module with $VREF$ output terminal.

6.5.2 Transresistances Placement

The Figure 6.15 shows the same IA layout from Figure 6.14, but the internal layout of amplifier modules is hidden. This illustration provides an easier mean to visualize the transistors used.

Located at the right side of $OPAMP\_A$, transistors $M3\_A$ and $M1\_A$ are placed next to the output terminal, while transistor $M2\_A$ is placed down to $M1\_A$. The last three components are located in the same position, but referenced to $OPAMP\_B$ module. Transistor $M3\_B$ is next to $M1\_B$, which is located below transistor $M2\_B$. The Figure 6.16 shows a closer view of $M3\_A$, $M1\_A$ and $M2\_A$ placement.

6.6 Signal Conditioning Circuit

The final layout is obtained from integrating the IA layout shown in Figure 6.14, the current-source load inverter layout from Figure 6.6, and the triple push-pull inverter layout from Figure 6.5, given as a result the layout design from Figure 6.17. The system layout as six terminal ports: *positive input* and *negative input* coming from the resonant microsensor, *system output*, V_{DD}, V_{SS}, and *ground* for reference.

The inverter modules are located between the output terminal of $OPAMP\_C$ and the polysilicon resistance, R_G. A detailed view of inverters layout placement is shown in Figure 6.18.

During every module design, a physical verification analysis using Calibre® from Mentor Graphics, was used to check for *design rules check* (DRC) and *short circuit* errors. Those tools help on finding fabrication process errors and undesirable layout connections [51]. The short circuit analysis showed no shorts in the layout. The DRC analysis showed some warnings related with fabrication layers missing on the layout (it was previously explained that some layers required for fabrication are not present during design, but can be automatically generated by the layout tool). Moreover, warnings related to the metal percentage of metal layers were showed by the DRC analysis. The layout tool can also fill the required surface automatically.

6.6.1 Summary

The sizes of the individual modules that comprise the core OTA layout are summarized in Table 6.1. The core OTA layout has a total surface of 165 $\mu m \times 82$ μm,

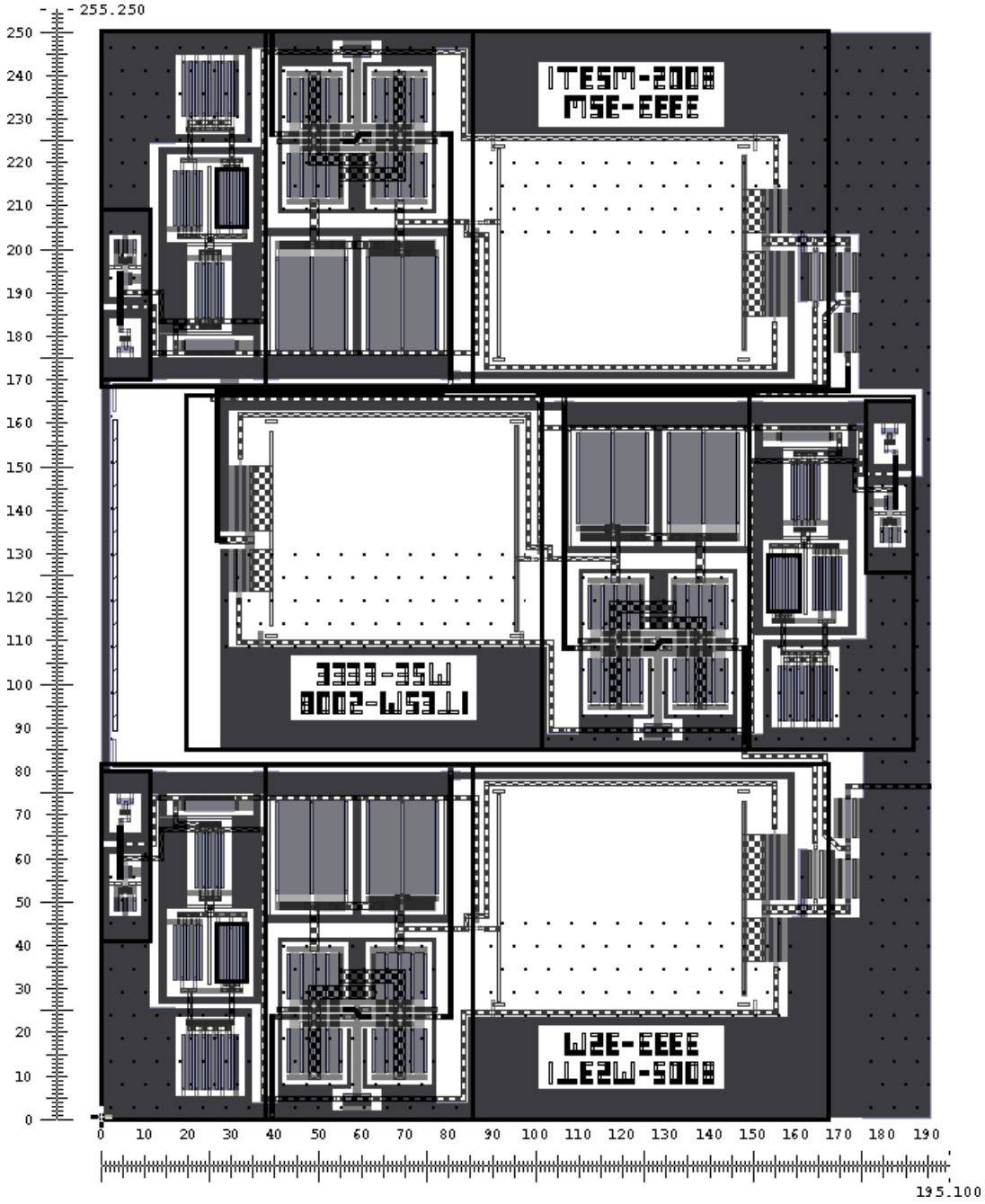

Figure 6.14: Layout of the IA circuit module.

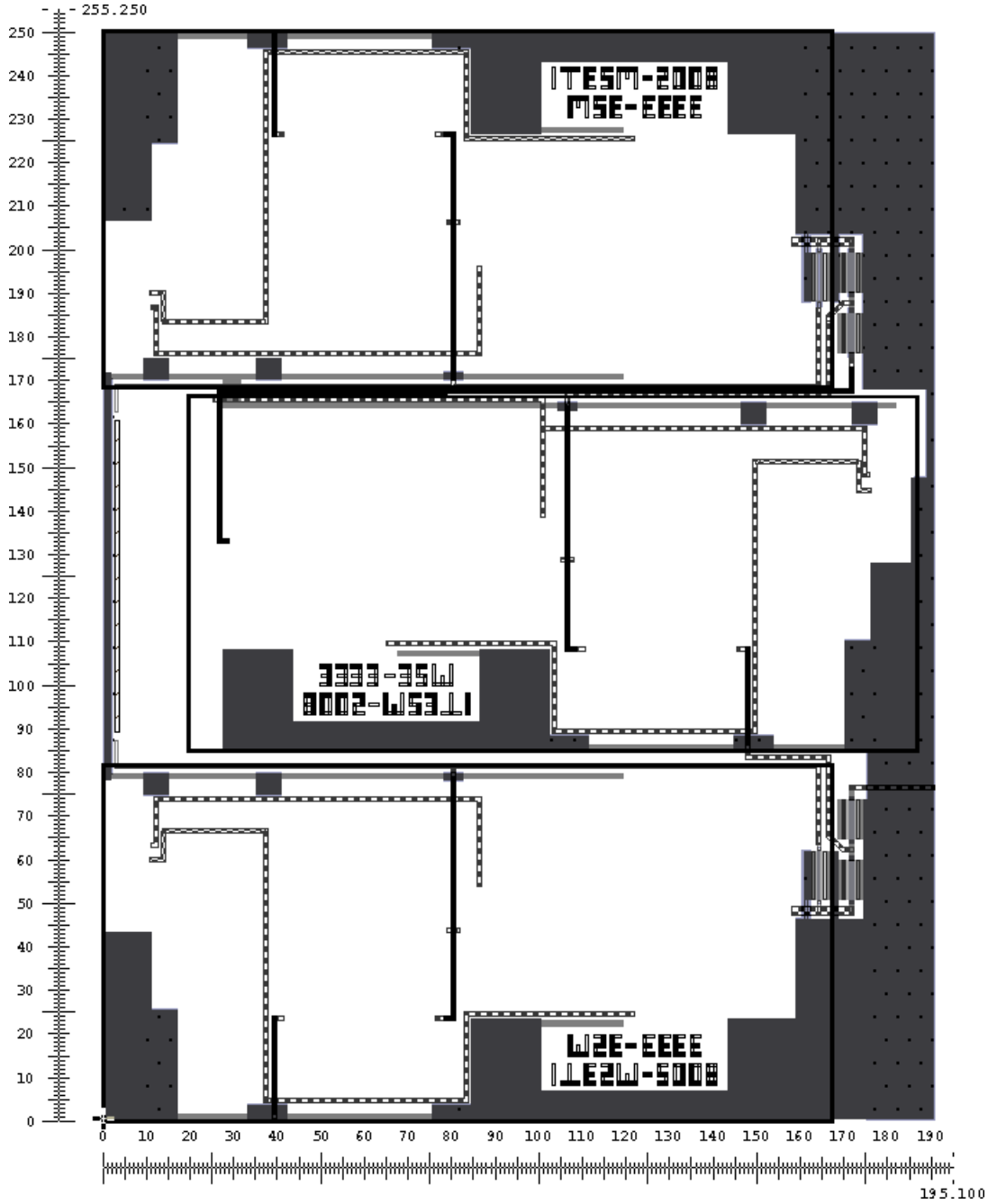

Figure 6.15: Simplified layout of the IA circuit module.

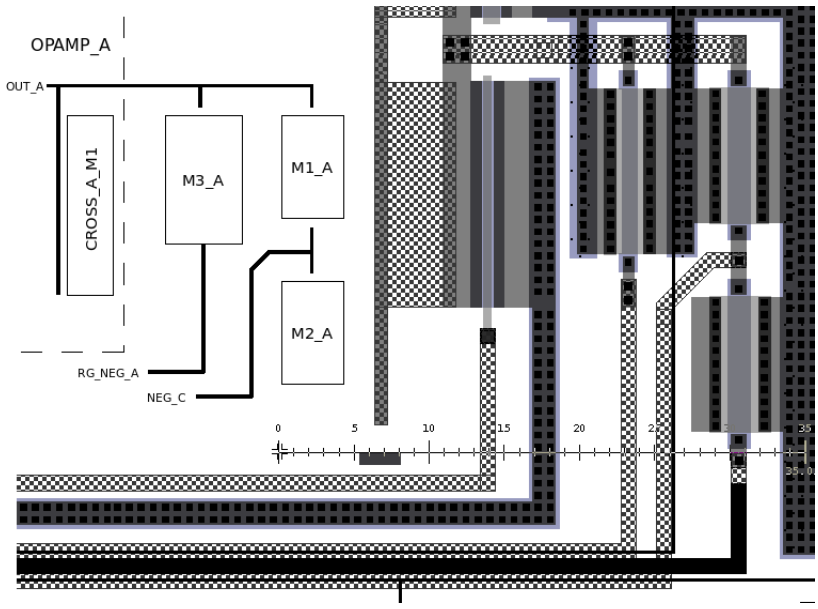

Figure 6.16: Closer view of the output mesh from $OPAMP\_A$ configured for the IA layout.

which is around 10 % of the layout surface used in related works [12]. This is because of other works intergate not only signal conditioning circuitry, but analog to digital converters , I/O ports, memory, a processor, and other digital blocks as well.

Table 6.1: OTA modules layout area

Module name	Length	Width
Differential-input module	42 μm	80 μm
Current-source load module	79 μm	59 μm
Bias voltage module	11 μm	38.5 μm
Bias current module	24.5 μm	80 μm

The total area of the instrumentation amplifier layout is 190 $\mu m \times 250$ μm. Compared to the surface layout of the inverter modules, shown in Table 6.2, the IA layout is much bigger than inverters layout.

The integrated modules of the complete system cover a surface layout of 190 $\mu m \times$ 250 μm, the same than the IA layout. The complete layout is surrounded by *metal1* shapes tied to the substrate forming the bulk connection.

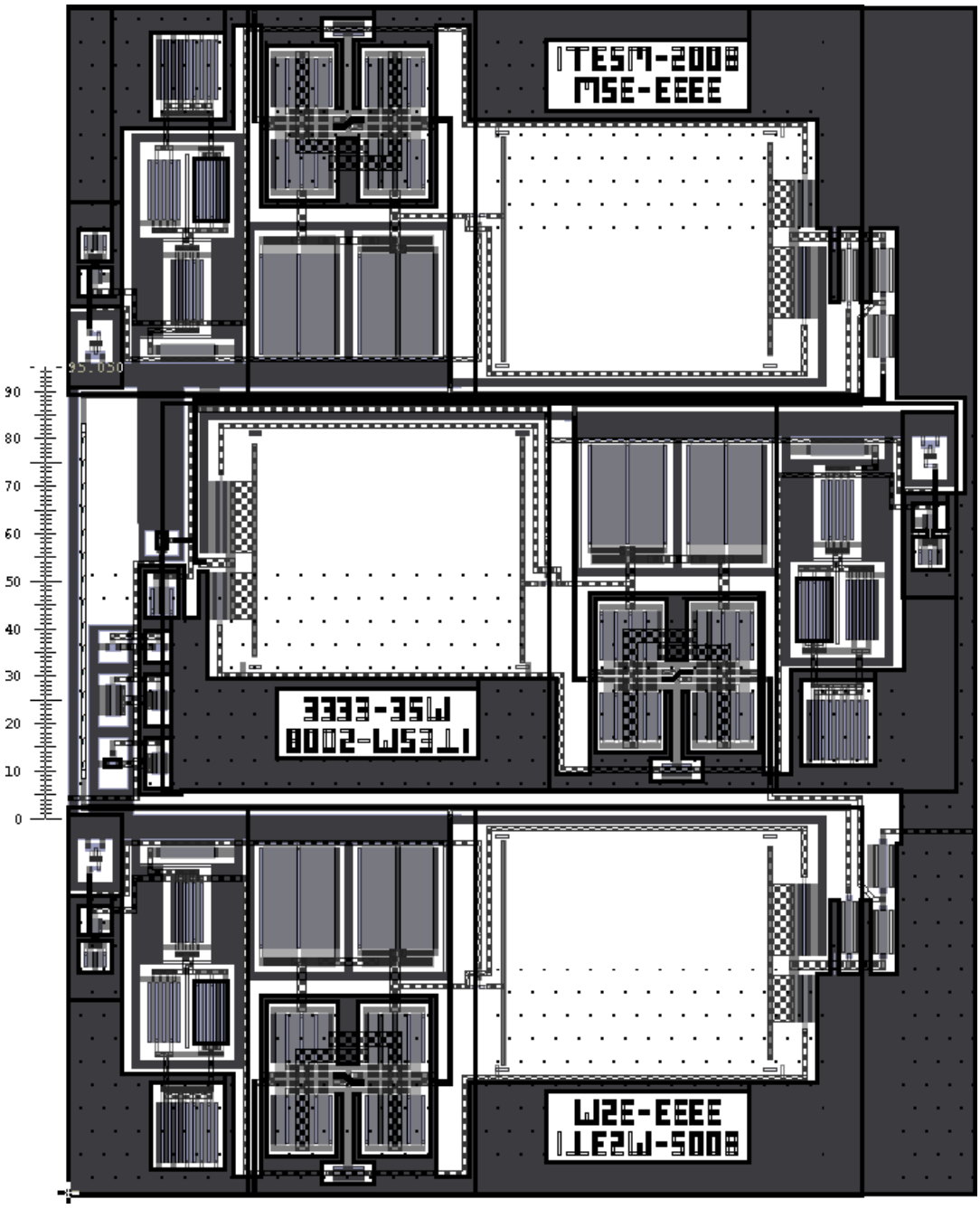

Figure 6.17: Layout design of the signal conditioning system.

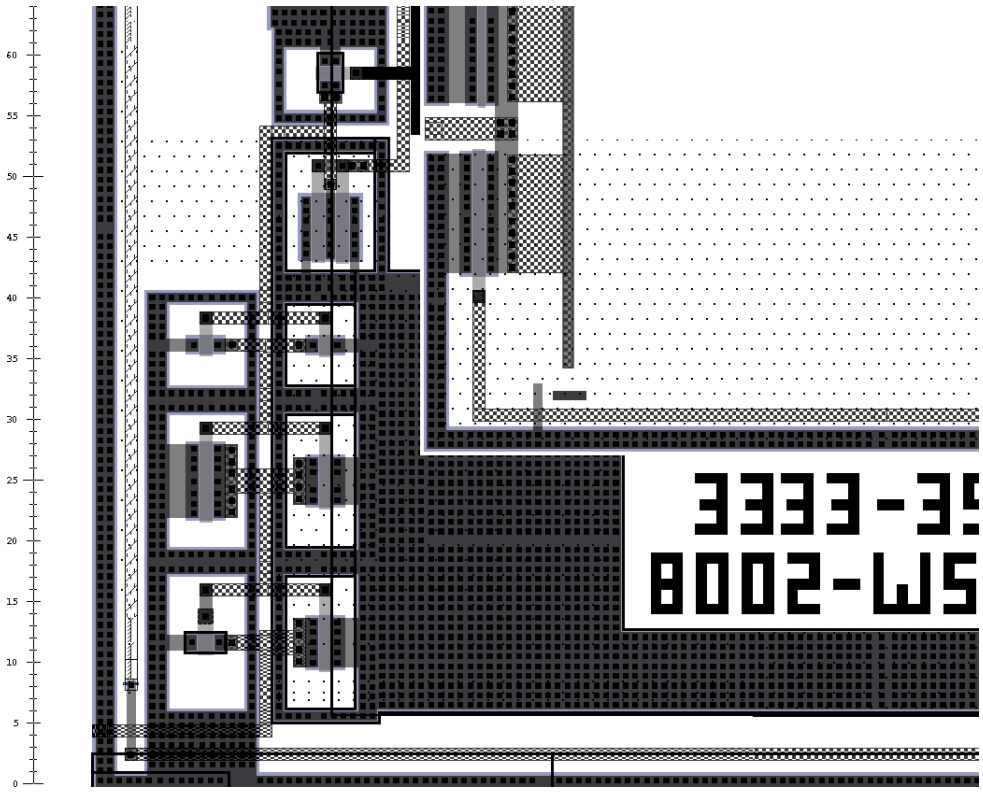

Figure 6.18: Closer view of the inverter modules placement from Figure 6.17.

Table 6.2: Inverter modules layout area

Module name	Length	Width
Current-source module	9.5 μm	22.5 μm
Push-pull A module	9.5 μm	19.35 μm
Push-pull B module	13.5 μm	19.35 μm
Push-pull C module	13.5 μm	19.35 μm

Chapter 7

Conclusions and Future Work

7.1 Conclusions

Recent progress in microelectromechanical systems is being applied to biomedical applications and has become a new field of research into itself, known as BioMEMS. Depending on the transducer mechanism, BioMEMS sensors allow the conversion of a specific magnitude to the electrical domain.

The aim of this thesis was the design of a CMOS microelectronic interface circuit, capable of measuring a voltage-frequency differential signal from a resonant microsensor. Simulations showed that the designed CMOS interface is able to monitor signals up to $V_{diff} = \pm 1\ \mu V_p$ oscillating at $f_{diff} = 100\ kHz$, giving at the output a $V_{out} = \pm 1.5V$ squarewave signal with a $f_{out} = f_{diff}$ frequency. The implemented methodology introduces a modular design for the circuit stages that conform the system. At the end, the final layout area of the microelectronic circuit, designed with the CMOS AMS® 0.35 μm technology process parameter libraries, is 250 $\mu m \times 190\ \mu m$.

Due to modularization methodology, both, a schematic circuit diagram and a layout were designed for each individual circuit stage. Moreover, a complete analysis of those stages is reported. Therefore, facilitating the reutilization of any module already designed into another different CMOS integrated circuit.

7.2 Future Work

This work has provided an initial effort to design an analog-to-digital stage of a complete CMOS *System on Chip* (SoC) integrated circuit. However, the design work has not finished yet. The requirements below need to be concluded before going for the fabrication process

- A simulation analysis considering the normal body temperature is required in order to continue on the layout design.
- Once verified the layout, a parasitic extraction (PEX) analysis is required, to verify the proper schematic circuit behavior that considers layout parasitic capacitances, and iterate for compensating any abnormal behavior as needed.
- The design of the final module including the pads and bound wires of the IC to external pins is pending, and shall be done before generation of fabrication process files.
- Some layers not required for the layout design, but required for the layout fabrication need to be generated. This is an automatic process, executed from ICstation® command line.
- Generate the process fabrication files by using ICstation® layout tool.
- Design a CMOS compatible MEMS resonant sensor, with the signal restrictions specified in this report.

Appendix A

Main Numerical Results of the Two-Stage OTA Design

The Table below shows the main numerical results obtained from g_m/I_D design methodology for the OTA.

p-channel input OTA all sizes are in [um]
numerical results obtained from gm/Id method.
simulation results obtained from Mentor graphics Icstudio by implementing 0.35 Austrimycrosystems process technology

	M1, M2			M3, M4			M5, M12			M6			M7			Numerical results					
graph	S	W	L	S	W	L	S	W	L	S	W	L	S	W	L	Cc [pF]	Rc [Kohm]	Av [V/V]	Av [dB]	P [uWatt]	Vo [V]
89	30	60	2	6	9	1.5	6.3	3	0.5	19.5	19.5	1	10.5	5.250	0.5	2.2	20.0588	9,597.7919	79.64	86.63	1.2390
90	30	60	2	8	16	2	6.3	6	1	22.5	22.5	1	8.85	4.425	0.5	2.2	20.0588	11,090.7818	80.90	79.41	1.2356
91	30	60	2	8	20	2.5	6.3	6	1	22.5	22.5	1	8.85	4.425	0.5	2.2	20.0588	11,090.7818	80.90	79.41	1.2356
92	30	60	2	8	24	3	6.3	6	1	22.5	22.5	1	8.85	4.425	0.5	2.2	20.0588	11,090.7818	80.90	79.41	1.2356
93ntype	30	60	2	8	24	3	6.3	6	1	22.5	22.5	1	8.85	4.425	0.5	2.2	20.0588				
94	30	60	2	6	42	7	6.3	6	1	22.5	22.5	1	8.85	4.425	0.5	2.2	20.0588	8,318.0863	78.40	94.88	1.1947
95	30	60	2	6	42	7	6.3	6	1	19.5	19.5	1	10.2	5.100	0.5	2.2	20.0588	9,597.7919	79.64	86.63	1.2352
96	30	60	2	6	42	7	6.3	6	1	22	22.0	1	9	4.500	0.5	2.2	20.0588	8,507.1338	78.60	93.50	1.2006
97	30	30	1	6	42	7	6.3	6	1	22	22.0	1	9	4.500	0.5	2.2	20.0588	8,507.1338	78.60	93.50	1.2006
98	30	75	2.5	6	42	7	6.3	6	1	22	22.0	1	9	4.500	0.5	2.2	20.0588	8,507.1338	78.60	93.50	1.2006
99	30	75	2.5	6	42	7	6.3	6	1	30	15.0	0.5	8	4.000	0.5	2.2	20.0588	6,238.5648	75.90	115.50	1.1292
100	30	75	2.5	6	42	7	6.3	6	1	30	15.0	0.5	7.5	3.750	0.5	2.2	20.0588	6,238.5648	75.90	115.50	1.1170
101	30	75	2.5	6	42	7	6.3	6	1	30	15.0	0.5	6.6	3.300	0.5	2.2	20.0588	6238.56	75.9	115.5	1.0918
102	30	75	2.5	6	42	7	6.3	6	1	30	15.0	0.5	10	5.000	0.5	2.2	20.0588	6,238.5648	75.90	115.50	1.1683
103	30	75	2.5	6	42	7	6.3	6	1	25	12.5	0.5	6.6	3.300	0.5	2.2	20.0588	7,486.2777	77.49	101.7500	1.1273
104	30	75	2.5	6	42	7	6.3	6	1	20	10.0	0.5	6.6	3.300	0.5	2.2	20.0588	9,357.8471	79.42	88.0000	1.1667
105	30	75	2.5	6	42	7	6.3	6	1	15	7.5	0.5	6.6	3.300	0.5	2.2	20.0588	7,407.4074	77.39	102.4820	1.1253
106	30	75	2.5	6	42	7	6.3	6	1	18	9.0	0.5	6.6	3.300	0.5	2.2	20.0588	8,888.8889	78.98	90.9017	1.1580
92	30	60	2	8	24	3	6.3	6	1	22.5	22.5	1	8.85	4.425	0.5	2.2	20.0588	11,090.7818	80.90	79.4062	1.2356
107	30	75	2.5	6	42	7	6.3	6	1	30	15.0	0.5	6.6	6.600	1	2.2	20.0588	6,238.5648	75.90	115.5000	1.0918
108	30	75	2.5	6	42	7	6.3	6	1	30	15.0	0.5	8	8.000	1	2.2	20.0588	6,238.5648	75.90	115.50	1.1292
109	30	75	2.5	6	42	7	6.3	6	1	30	15.0	0.5	15.5	15.50	1	2.2	20.0588	6,238.5648	75.90	115.50	1.2336
110	30	75	2.5	6	42	7	6.3	6	1	30	15.0	0.5	10	10.00	1	2.2	20.0588	6,238.5648	75.90	115.5000	1.1683
111	30	75	2.5	6	42	7	6.3	6	1	30	15.0	0.5	9	9.000	1	2.2	20.0588	6,238.5648	75.90	115.50	1.1504
112	30	75	2.5	6	42	7	6.3	6	1	30	15.0	0.5	9.5	9.500	1	2.2	20.0588	6,238.5648	75.90	115.50	1.1597
113	30	75	2.5	6	42	7	6.3	6	1	19.4	9.7	0.5	9.8	9.800	1	2.2	20.0588	9,613.6976	79.66	86.54	1.2301
114	30	75	2.5	6	42	7	6.3	6	1	30	15.0	0.5	9.9	9.900	1	2.2	20.0588	6,238.5648	75.90	115.50	1.1667

Figure A.1: Fragment of the design iterations record by applying g_m/I_D methodology, part A.

	simulation results							
graph	Av [dB]	F(-3) [Khz]	Ph (-3db)	F [Mhz]	Ph (0dB)	Inoise [uA]	Onoise [mA]	
89	69.30490	2.47989	-44.89233	8.06365	-96.70586	2.27914	6.65299	M7 in nonsaturation region
90	73.42617	1.63295	-44.47034	7.67263	-102.50226	1.51483	7.10678	M7 in nonsaturation region
91	69.57435	2.46243	-44.87693	7.23876	-103.77062	1.19103	3.58624	M7 in nonsaturation region
92	68.11863	2.83507	-44.75260	6.92231	-105.42648	0.98289	2.50287	M7 in nonsaturation region. gain is in the limit
93ntype	92.60417	0.25657	-44.80975	6.73345	-120.68540	0.77281	32.98252	testin n-channel input with p-channel ratios. all saturated
94	89.70718	0.26978	-44.77572	6.61816	-116.26729	0.47452	14.50832	suggestions for M6, M7 NOT used. all saturated. pole3 iss
95	66.61692	3.11119	-44.48898	5.75687	-113.05995	0.47453	1.01649	M7 in nonsaturation region
96	83.79599	0.52438	-44.82301	6.30134	-115.78073	0.47452	7.34612	all saturated
97	78.60029	0.93834	-44.78429	6.46954	-114.75798	0.61223	5.21112	all saturated. by decreasing L1, INOISE increases
98	84.68044	0.47459	-44.79541	6.48913	-116.77786	0.45545	7.80651	
99	90.59825	0.24428	-44.85140	6.80407	-113.60683	0.45546	15.43006	
100	91.27652	0.22635	-44.76370	6.74323	-114.20539	0.45546	16.68324	
101	92.07523	0.20679	-44.86271	6.44532	-115.22829	0.45546	18.29007	error during running script(see numerical gain)
102	73.14829	1.65	-44.82660	6.79440	-109.52319	0.45546	2.06953	M7 in nonsaturation region. suggestions from method not
103	90.78165	0.23909	-44.80455	5.98153	-118.26951	0.45547	15.75956	all saturated
104	74.46205	2.43807	-44.76111	5.20710	-120.83776	0.45548	2.40754	M7 in nonsaturation region
105	65.39870	3.47316	-44.79821	4.23729	-124.81380	0.45550	0.84805	M7 in nonsaturation region
106	69.82600	2.29741	-44.76490	4.81583	-121.96926	0.45547	1.41181	M7 in nonsaturation region
92	68.11863	2.83507	-44.75260	6.92231	-105.42648	0.98289	2.50287	M7 in linear. Final design
107	95.85197	0.13442	-44.78317	6.41450	-114.78179	0.45546	28.25205	M7 in nonsaturation region. gain is in the limit
108	79.82590	0.81260	-44.88111	6.89001	-111.58132	0.45546	4.46425	M7 in nonsaturation region
109	60.00720	5.39405	-44.76632	5.92021	-97.77270	0.45546	0.45584	M7 in nonsaturation region
110	67.68264	2.82291	-44.74779	6.59812	-106.36714	0.45546	1.10303	M7 in nonsaturation region
111	71.09066	2.03065	-44.88570	6.73523	-108.55084	0.45546	1.63300	M7 in nonsaturation region
112	69.14750	2.45601	-44.86861	6.66564	-107.40139	0.45546	1.30566	M7 in nonsaturation region
113	68.22713	2.68239	-44.78471	6.62473	-106.76945	0.45546	1.17438	M7 in nonsaturation region
114	67.94887	2.75358	-44.75703	6.61139	-106.56663	0.45546	1.13736	M7 in nonsaturation region

Figure A.2: Fragment of the design iterations record by applying g_m/I_D methodology, part B.

Appendix B

Scripts Used for Design Methodology

The following programs were codified in order to make organized, accurate, and fast numerical calculations during the two-stage OTA design. These scripts were developed for *GNU Octave*, version 2.9.9 [46].

B.1 Octave Script for OTA Stage Design

```
% pdiff1.m obtained from final_pdiff_second_st.m
% created by Luis Saracho, on sept-10-2007
% last updated on march-18-2008
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
% this code is based on process parameters of the p-type, n-type models of Allen and
% Holberg book, cmos analog circuit design, 2nd edition. it follows the procedure of
% table 6.3-2 (pag. 274) for the two-stage unbuffered opamp, according to section
% 6.3 (pag. 269), but it is adjusted for a p-type input pair. perfect matching is
% assumed: gm1=gm2=gm_i, gm6=gm_ii, gds2+gds4=g_i, gds6+gds7=g_ii
% current of second stage, n-type transistor is defined by two different methods and
% the greatest is selected. there is included a code section for determining nulling
% resistor value.

% clear memory
% clear all;
% close all;
%*************** input data from p-type process parameters (pag. 75, pag. 93)
av = 5000;       % [V/V] minimum dc-gain
```

```
cl_b = 10;      % [picofaradios] charge capacitance
gb_b = 2;        % [MHz] unity-gain bandwidth
kp = 50; % [uA/volts^2] p-type transconductance parameter
kn = 110; % [uA/volts^2] n-type transconductance parameter
pdiss_b = 2;     % [mWatts] maximum specified power dissipation
sr_b = 5;       % [volts/useg] maximum slew rate
tox =140*10^-10; % [meters] thickness of gate oxide
ts_b = 1;        % [useg] maximum specified sletting time
vdd = 1.5;       % [volts] most positive circuit reference
vin_max = 0.3;     % [volts] maximum input common mode voltage
vin_min = -0.3;    % [volts] minimum input common mode voltage
vout_max = 0.8;    % [volts] maximum output voltage
vout_min = -0.8;   % [volts] minimum output voltage
vss = -1.5;      % [volts] most negative circuit reference
vtn = 0.7;   % [volts] n-type threshold voltage
vtn_max = vtn + 0.15;   % definition of maximum n-type threshold voltage
vtn_min = vtn - 0.15;   % definition de minimum n-type threshold voltage
vtp = -0.7;   % [volts] p-type threshold voltage
vtp_max = vtp - 0.15;   % definition of maximum p-type threshold voltage
vtp_min = vtp + 0.15; % definition of minimum p-type threshold voltage

%*************** code labels
% cc        ota compensation capacitance
% cgs3      gate_source parasitic capacitance of M3
% cox_p     thickness of gate oxide for p-type transistor
% gm1       transconductancce of M1
% gm2       transconductancie of M2
% gm3       transconductancie of M3
% gm4       transconductancie of M4
% gm6       transconductancie of M6
% i5        drain current of M5
% i6        drain current of M6
% l_1       length of transistor M1 [meters]
% l_2       length of transistor M2 [meters]
% l_3       length of transistor M3 [meters]
% l_4       length of transistor M4 [meters]
% l_5       length of transistor M5 [meters]
% l_6       length of transistor M6 [meters]
% l_7       length of transistor M7 [meters]
% l_8       length of transistor M8 [meters]
% s1        aspect ratio, W/L, of M1
```

```
% s2        aspect ratio, W/L, of M2
% s3        aspect ratio, W/L, of M3
% s4        aspect ratio, W/L, of M4
% s5        aspect ratio, W/L, of M5
% s6        aspect ratio, W/L, of M6
% s7        aspect ratio, W/L, of M7
% s8        aspect ratio, W/L, of M8
% vds5_sat  D-S saturation voltage of M5
% vds7_sat  D-S saturation voltage of M7
% vgg6      gate voltage of M6
% vsg6      S-G voltage of M6
% w_1       transistor width of M1 [meters]
% w_2       transistor width of M2 [meters]
% w_3       transistor width of M3 [meters]
% w_4       transistor width of M4 [meters]
% w_5       transistor width of M5 [meters]
% w_6       transistor width of M6 [meters]
% w_7       transistor width of M7 [meters]
% w_8       transistor width of M8 [meters]

%*************** parameters assignation
eo_b = 8.854*10^-14;    % free-space permitivity [farad/cm]
k1_b = kp;
k3_b = kn;
k4_b = kn;
k5_b = kp;
k6_b = kn;
k7_b = kp;
k8_b = kn;
k9_b = kp;
k10_b = kn;
k11_b = kn;
k12_b = kp;

lambda_n = 0.04; % [1/volts] for L=1um
lambda_p = 0.05; % [1/volts] for L=1um
vt1 = vtp;
vt3 = vtn;
vt6 = vtn;
vt8 = vtn;
vt10 = vtn;
```

```
w_base = 0.5*10^-6; % base width of transistor [meters]
l_base1 = 0.5*10^-6; % base length of transistor [meters]
l_base2 = 1*10^-6;
l_base3 = 2.5*10^-6;
l_base4 = 7*10^-6;

% final lenghts, defined after several iterations
%l_1 = l_base3;
%l_2 = l_base3;
%l_3 = l_base4;
%l_4 = l_base4;
%l_5 = l_base2;
%l_6 = l_base1;
%l_7 = l_base2;
%l_8 = l_base1;
%l_9 = l_base2;
%l_10 = l_base1;
%l_11 = l_base1;
%l_12 = l_base2;
%%%%%%%%%%
% first lenghts value. for debugging this design
l_1 = l_base2;
l_2 = l_base2;
l_3 = l_base2;
l_4 = l_base2;
l_5 = l_base2;
l_6 = l_base2;
l_7 = l_base2;
l_8 = l_base2;
l_9 = l_base2;
l_10 = l_base2;
l_11 = l_base2;
l_12 = l_base2;

%*************** change of units
cl = 10e-12;
cl = cl_b * 1 * 10^-12;     % conversion of cl to [faradios]
eo = eo_b * 100;            % conversion of eo to [faradios/metro]
gb = gb_b * 1 * 10^6;       % conversion of gb to [Hz]
k1 = k1_b * 1 * 10^-6;      % conversion of k1 to [amp/volts^2]
```

```
k3 = k3_b * 1 * 10^-6;      % conversion of k3 to [amp/volts^2]
k4 = k4_b * 1 * 10^-6;      % conversion of k4 to [amp/volts^2]
k5 = k5_b * 1 * 10^-6;      % conversion of k5 to [amp/volts^2]
k6 = k6_b * 1 * 10^-6;      % conversion of k6 to [amp/volts^2]
k7 = k7_b * 1 * 10^-6;      % conversion of k7 to [amp/volts^2]
k8 = k8_b * 1 * 10^-6;      % conversion of k8 to [amp/volts^2]
k9 = k9_b * 1 * 10^-6;      % conversion of k9 to [amp/volts^2]
k10 = k10_b * 1 * 10^-6;    % conversion of k10 to [amp/volts^2]
k11 = k11_b * 1 * 10^-6;    % conversion of k11 to [amp/volts^2]
k12 = k12_b * 1 * 10^-6;    % conversion of k12 to [amp/volts^2]
pdiss = pdiss_b * 1 * 10^-3;% conversion of pdiss to [Watts]
sr = sr_b * 1 * 10^6;       % conversion of sl to [v/seg]
ts = ts_b * 1 * 10^-6;      % conversion of ts to [seg]
vt1_min = vtp_min;          % definition of minimum threshold voltage for M1
vt1_max = vtp_max;          % definition de maximum threshold voltage for M1
vt3_max = vtn_max;          % definition de maximum threshold voltage for M3

%*************** introduction
clc;
fprintf('\ndifferential p-type input pair two-stage amplifier design');
fprintf('\ninput parameters:');
fprintf('\nminimum voltage gain,  Av=%6f V/V',av);
fprintf('\npositive supply,             Vdd=%3.4f Volts',vdd);
fprintf('\nnegative supply,            Vss=%3.4f Volts',vss);
fprintf('\nunity-gain bandwidth,    GB=%9.3f Hz  ',gb);
fprintf('\ncharge capacitance,      Cl=%3.4e Faradios',cl);
fprintf('\nslew rate,                    SR=%3.4e V/seg',sr);
fprintf('\noutput voltage,             Vout=%3.4f Volts a %3.4f Volts
\n', vout_min, vout_max);
fprintf('\ninput voltage,                ICMR=%3.4f Volts a %3.4f Volts
\n', vin_min, vin_max);
fprintf('\ndissipation power,         Pdiss=%3.4e Watts',pdiss);

%*************** obtaining compensation capacitance value
cc = 0.22 * cl;
fprintf('\n\nthe minimum compensation capacitance calculated, Cc =%3.4e F',cc);
fprintf('\nwhich is the minimum value for ensuring compensation:
\nCc_min = 0.22*C_charge \n')

%*************** option of changing obtained value of Cc
opc = input('do you want to change compensation capacitance (y/n)?? ','y');
```

```
if (opc=='y') | (opc=='Y')
    fprintf('input new Cc value (in Farads, example: 2 uFarads = 2e-6 Farads) \n');
    cc = input('>>> ');
    fprintf('new compensation capacitance value, Cc=%3.4e Farads',cc);
end;

%*************** define differential pair current
i5 = sr * cc;
fprintf('\n \nfor M5, calculated current source is, I5= %3.4e Amperes', i5);

%*************** define aspect ratio of M3, M4
s3 = i5 / ( k3 * ((-vss + vin_min - vt3_max + abs(vt1_min) )^2) );
%s3=6; %%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
s4 = s3;
fprintf('\n \nfor the current mirror, aspect ratio of M3 is, S3 = %3.4f adim.
\nsame value is for M4, S4= %3.4f adim.',s3, s4);
if (s3 < 1)
    fprintf('\nM3 aspect ratio must be greater than unity.
\nfor M3, S3= %3.4f adim. \nit is required to calculate again \n',s3);
    opc = input('program will continue running. press enter, follow instructions..');

%*************** option of changing aspect ratio S3, S4
    opc = input('do you want to change aspect ratio of M3 and M4 (y/n)?? ','y');
    if (opc=='y') | (opc=='Y')
        fprintf('input new value of S3 (S3=W3/L3, non-dimensional) \n');
        s3 =input('>>> ');
        s4 = s3;
        fprintf('new aspect ratio of M3 and M4, S3=S4=%3.4f adim.', s3);
    end;
end;

%*************** verify that pole3 of the system is greater than 10*gbp
gm3 = sqrt( 2 * k3 * (i5/2) * s3)
w_3 = s3 * l_3;         %***** width of M3 [meters]
eox = 3.9*eo;           %***** eox, silicon dioxide permitivity [farads/meters]
cox = eox / tox
cgs3 = (2/3) * w_3 * l_3  * cox
p3 = gm3 / (2 * cgs3);
fprintf('\nvalue of pole3 is p3= %3.4e rad/seg', p3);
p3_hz = p3 / (2*pi)    %***** conversion of p3 from [rad/segs] to [Hz]
fprintf('\n \nverification of mirror pole, p3, as reference of circuit stability');
```

```
if ( p3_hz  >  10*gb )
    fprintf('\ngood: the pole and zero generated by Cgs3 & Cgs4 are not dominant
\nbecause of p3>>10GB, %3.4e Hz > %3.4e Hz', p3_hz,(10*gb));
else
    fprintf('\nwarning: there is an issue with p3, since it does not comply with
\np3>10GB, %3.4e Hz < %3.4e Hz \n', p3_hz,(10*gb));
    opc = input('program will continue. press enter and follow the instructions..');
end;

%*************** define aspect ratio of M1 & M2
gm1 = (gb*2*pi) * cc;
s1 = (gm1^2) / (k1*i5);  %***** note: i5=2*i1
gm2 = gm1;
s2 = s1;
fprintf('\n \nfor input transistors, M1 and M2 \ncalculated transconductance of M1
\nand M2, gm1=gm2= %3.4e Siemens \naspect ratio of M1 and M2,
\nS1=S2= %3.4f adim. \n', gm1, s1);

%*************** option of changing aspect ratio S1, S2
opc = input('do you want to change aspect ratio of M1 and M2 (y/n)?? ','y');
if (opc=='y') | (opc=='Y')
    fprintf('input new value of S1 (S1=W1/L1, non-dimensional) \n');
    s1 =input('>>> ');
%    s1 = 30; %%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
    s2 = s1;
    fprintf('new aspect ratio of M1 and M2, S1=S2=%3.4f adim.', s1);
end;

%*************** aspect ratio of M5 from maximum saturation voltage
vds5_sat = vdd - vin_max - sqrt(i5/(k1*s1)) - abs(vt1_max);
s5 = (2*i5) / ( k5 * vds5_sat^2 );
%s5=6.3; %%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
fprintf('\n \nfor transistor M5 \nsaturation voltage, Vds= %3.4f Volts
\naspect ratio of M5, S5= %3.4f adim. \n', vds5_sat, s5);

%*************** option of changing aspect ratio S5
opc = input('do you want to change aspect ratio of M5 (y/n) ?? ','y');
if (opc=='y') | (opc=='Y')
    fprintf('input new value of S5 (S5=W5/L5, non-dimensional) \n');\
    s5 =input('>>> ');
    fprintf('new aspect ratio of M5, S5= %3.4f adim.', s5);
```

```
end;

%*************** define parameters of M4 and M6
fprintf('\n \nfor transistors M4, M6');
gm4 = sqrt( 2 * k4 * (i5/2) * s4)
gm6 = 2.2 * gm2 * ( cl/cc );

%*************** option of changing gm6 for gm6 = 10*gm1
if ( gm6 < (10*gm1) )
    fprintf('\nwarning: transconductance value of M6, gm6, does not comply with
\n phase margin of 60degrees, condition gm6 > 10*gm1 does not accomplish
\ngm1 = %3.4e Siemens \ngm6 = %3.4e Siemens \n', gm1, gm6);
opc=input('do you wnat to change value of gm6 for gm6=10*gm1 (y/n) ?? ','y');
    if (opc=='y') | (opc=='Y')
        gm6 = ( 10 * gm1 );
        fprintf('new transconductance value of M6, gm6=%3.4e Siemens \n',gm6);
     end;
end;

s6 = s4 * ( gm6/gm4 );
%s6=30; %%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
i6_1 = (gm6^2) / (2 * k6 * s6);
i6_2 = ( s6 / s4 ) * ( i5 / 2 );
fprintf('\ntransconductance of M4, gm4= %3.4e Siemens \ntransconductance of
\mM6, gm6= %3.4e Siemens \naspect ratio of M6, S6= %3.4f adim.
\nfrom transconductance, the current is defined as, I6a=%3.4e Amperes from
\nmirror, the current is defined as, I6b=%3.4e Amper \n',gm4,gm6,s6,i6_1,i6_2);

%*************** option of changing aspect ratio of M6
opc = input('do you want to change aspect ratio of M6 (y/n)?? ','y');
if (opc=='y') | (opc=='Y')
    fprintf('input new value of S6 (S6=W6/L6, non-dimensional) \n');
    s6 =input('>>> ');
    fprintf('new aspect ratio of M6 S6=%3.4f adim.', s6);
    i6_1 = (gm6^2) / (2 * k6 * s6);
    i6_2 = ( s6 / s4 ) * ( i5 / 2 );
    fprintf('\nadjust M6 currents to new aspect ratio of M6, S6=%3.4f adim.
\nI6a=%3.4e Amperes \nI6b=%3.4e Amperes', s6, i6_1, i6_2);
end;

%*************** obtaining maximum current I6
```

```
i6 = max( i6_1, i6_2 );

%*************** obtaining saturation voltage of M6
vds6_sat = (gm6 / (k6 * s6)); % vds[sat] = vgs-vt
fprintf('\ncurrents I6a, I6b shall be almost the same, I6a shall be greater
\nthan I6b though. otherwise there is a design issue regarding to M6.
\nselected value for current of M6, I6=%3.4e Amperes',i6);

%*************** define aspect ratio of M7
s7 = (i6/i5) * s5;
%s7=9.8;    %%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
fprintf('\n \nfor M7, the value of its aspect ratio is, S7=%3.4f adim. \n',s7);

%*************** option of changing aspect ratio of M7
opc = input('do you want to change aspect ratio of M7 (y/n)?? ','y');
if (opc=='y') | (opc=='Y')
    fprintf('input new value of S7 (S7=W7/L7, non-dimensional) \n');
    s7 =input('>>> ');
    fprintf('new aspect ratio of M7, S7= %3.4f adim.', s7);
end;

%*************** define aspect ratio of M12
s12 = s5;
fprintf('\n \nthe aspect ratio for transistor M12 is the same than for transistor M5,
\nS12=S5=%3.4f adim.',s12);
fprintf('\nthus, current specified in the current source is the same than I5 (current
\nmirror between M12 and M5)');

%*************** verify minimum output voltage
vgs6 = vds6_sat + vt6;;
fprintf('\n \nminimum output voltage requirement for the circuit,
\nvout_min=%3.4f Volts gate to source voltage of M6, Vgs6=%3.4f Volts
\n',vout_min, vgs6);
if (vgs6 < vout_min)
    fprintf('\nwarning: design issue. output voltage does not comply with minimum
\nvoltage requirement \nsince Vout_min < Vgs6');
end;

%*************** verify maximum output voltage
vsd7_sat =  sqrt( (2 * i6) / (k7 * s7) );
vmax = vdd - vsd7_sat;
```

```
fprintf('\n \nrmaximum output voltage requirement for the circuit,
\nvout_max=%3.4f Volts \nsource to drain voltage of M7, Vsd7=%3.4f Volts
\ncalculated maximum output voltage, Vmax=%3.4f',vout_max,vsd7_sat,vmax);
if (vout_max < vmax)
    fprintf('\nwarning: design issue. output voltage does not comply with maximum
\nvoltage requirement \nsince Vmax_calculado > Vout_max');
end;

%*************** output voltage range
fprintf('\n \nrequired output voltage range: %3.4f Volts < Vout < %3.4f Volts
\n', vout_min, vout_max);
fprintf('\ncalculated output range: %3.4f Volts < Vout < %3.4f Volts',vgs6,vmax);

%*************** calculate circuit dissipated power y and compare value with
% requirement
pd = (i5 + i6) * (vdd + abs(vss));
fprintf('\n \ndissipated power requirement, pdiss=%3.4e Watts
\ndissipated power calulated, pd=%3.4e Watts', pdiss, pd);
if (pd > pdiss)
    fprintf('\nwarning: design issue. dissipated power is greater than requirement');
end;

%*************** calculate circuit gain and compare with requirement
lambda2 = lambda_p;
lambda3 = lambda_n;
lambda6 = lambda_n;
lambda7 = lambda_p;
gan = (2 * gm2 * gm6) / (i5 * (lambda2+lambda3) * i6 * ( lambda6+lambda7));
gan_db = 20 *log10( gan );
av_db = 20 * log10( av );   % conversion of gain to [dB]
fprintf('\n \ngain required, av=%4.4f V/V \ncalculated gain, gan=%4.4f V/V
\n', av, gan);
fprintf('\nin decibels, Av=%4.4e dB \ncalculated    gan=%4.4e dB', av_db,gan_db);
if ( gan < av )
    fprintf('\nwarning: design issue. circuit gain is less than requirement');
end;

%*************** calculating transistors width
w_1 = s1 * l_1;         %***** width of M1 [meters]
w_2 = s2 * l_2;         %***** width of M2 [meters]
w_3 = s3 * l_3;         %***** width of M3 [meters]
```

```
w_4 = s4 * l_4;         %***** width of M4 [meters]
w_5 = s5 * l_5;         %***** width of M5 [meters]
w_6 = s6 * l_6;         %***** width of M6 [meters]
w_7 = s7 * l_7;         %***** width of M7 [meters]
w_12 = s12 * l_12;      %***** width of M12 [meters]

fprintf('\n \naspect ratio of transistors. given a specified length, every
\ncomponent width is obtained');
fprintf('\ntransistor  aspecto ratio     width          length');
fprintf('\n     M1        %3.4f              %3.4e        %3.4e',s1, w_1, l_1);
fprintf('\n     M2        %3.4f              %3.4e        %3.4e',s2, w_2, l_2);
fprintf('\n     M3        %3.4f              %3.4e        %3.4e',s3, w_3, l_3);
fprintf('\n     M4        %3.4f              %3.4e        %3.4e',s4, w_4, l_4);
fprintf('\n     M5        %3.4f              %3.4e        %3.4e',s5, w_5, l_5);
fprintf('\n     M6        %3.4f              %3.4e        %3.4e',s6, w_6, l_6);
fprintf('\n     M7        %3.4f              %3.4e        %3.4e',s7, w_7, l_7);
fprintf('\n     M12      %3.4f              %3.4e       %3.4e',s12, w_12, l_12);

%*************** calculate RHP zero compensation resistance
rz_1 = ( 1/gm6 ) * ( ( cc+cl ) / cc );
rz_2 = ( ( cc+cl ) / cc ) * ( 1 / sqrt( 2 * k6 * s6 * i6 ) );
fprintf('\n \ncalculate RHP zero compensation resistance
\nby using transconductance gm6, Rz_1 = %3.4e Ohms
\nby using current i6, Rz_2 = %3.4e Ohms', rz_1, rz_2);
rz = max(rz_1, rz_2);
fprintf('\nselected RHP zero compensation resistance, rz = %3.4e Ohms',rz);
fprintf('\n \n');
%   s1 w1 l1 s3 w3 l3 s5 w5 l5 s6 w6
%   l6 s7 w7 l7 cc rz av av_dB pd vmax
fprintf('%3.4f %3.4f %2.2f %3.4f %3.4f %2.2f %3.4f %3.4f %2.2f %3.4f %3.4f
\n%2.2f %4.4f %5.5f %2.2f %2.3f %3.4f %6.6f %2.3e %3.4f %3.4f', s1,
w_1*(10^6), l_1*(10^6), s3, w_3*(10^6), l_3*(10^6), s5, w_5*(10^6),
l_5*(10^6), s6, w_6*(10^6), l_6*(10^6), s7, w_7*(10^6), l_7*(10^6),
cc*(10^12), rz/1000, gan, gan_db, pd*(10^6), vmax);
fprintf('\n \nend of stage A.. \n');
input('press enter to continue..');
```

B.2 Octave Script for Bias Voltage Stage Design

```
% resist1.m obtained from final_null_resistor.m
% created by Luis Saracho, on sept-29-2007
% last updated on march-19-2008
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
% this program defines aspect ratios of transistors M8, M9, M10, M11, from the
% new block used for RHPzero compensation resistance biasing circuit. the obtained
% block is applied to the two-stage CMOS OTA design.

%data from Allen and Holberg book, pag.280
%cc =  3.0000e-12;
%cl =  1.0000e-11;
%gm6 =  942.5e-06;
%i5 =  3.0000e-05;
%i6 =  95.000e-06;
%i11 = 15.000e-06;
%k8 =  50.000e-06;
%k10 = 50.000e-06;
%s5 =  4.5000;
%s6 =  94;
%vt8 =  0.70000;
%vt10 =  0.70000;

% data from model of 68 dB. obtained from final_diff_second_st.m
cc =  2.2e-12;
cl =  10e-12;
gm6 =  276.46e-6;
i5 =  11e-6;
i10 = 5e-6;
i9 = i10;
i11 = i10;
i6 =  27.5e-6;
k8 =  110e-6;
k10 =  110e-6;
rz = 20058.784150011601;
s5 =  6.3000;
s6 =  30;
s10 = 1;
vt10 =  0.7;
```

```
%*************** length of transistors
w_base = 0.5*10^-6; % base width of transistor [meters]
l_base1 = 0.5*10^-6; % base length of transistor [meters]
l_base2 = 1*10^-6;
l_base3 = 2.5*10^-6;
l_base4 = 7*10^-6;

l_8 = l_base1;
l_9 = l_base2;
l_10 = l_base1;
l_11 = l_base1;
l_12 = l_base2;

%*************** define p2 pole to be a nulified
p2 = - gm6 / cl;
fprintf('\naccording to charge Cl=%3.4e Farads and to transconductance
\ngm6=%3.4e Siemens
\nsystem pole, p2, to be nulified is defined as, p2=%3.6e Rad/Seg', cl, gm6, p2);

%*************** equate zero to the pole that will be eliminated and define
% compensation resistance value
z1 = p2;
rz_3 = inv( gm6 ) - inv( z1 * cc );
delta_rz = abs( rz - rz_3 );

fprintf('\naccoding to p2 pole, zero is defined as z1=%3.6e Rad/Seg
\nhaving z1 compensation resistance is calculated, Rz=%3.4e Ohm', z1, rz_3);
fprintf('\nlast value of compensation resistance was Rz=%3.4e Ohm the difference
\nbetween the last and current value calculated is DeltaRz=%3.4f Ohm', rz, delta_rz);
rz = rz_3;
fprintf('\nthe new value of resistance will be used Rz=%3.4e Ohm', rz);

%*************** define aspect ratio of transistor M10. establishing S10 as unity, S10 = 1
fprintf('\n for transistor M10: established drain current, id10=%3.4e Amperes
\nestablished aspect ratio, S10=%3.4f Adim.', i10, s10);

%*************** option for changing aspect ratio S10
fprintf('\n');
opc = input('do you want to modify aspect ratio of M10 (y/n) ?? ','y');
if (opc=='y') | (opc=='Y')
    fprintf('input new value of S10 (S10=W10/L10, non-dimensional) \n');
```

```
    s10 = input('>>> ');
    fprintf('new aspect ratio of M11 S10=%3.4f Adim.', s10);
end;

%*************** define voltage Vgs_10
vgs10 = sqrt( ( 2 * i10 ) / ( k10 * s10 ) ) + vt10;
fprintf('\ngate to source voltage of M10, Vgs_10=%3.4f Volts', vgs10);

%*************** assume node A, node B of same voltage ( V_A = V_B ) then apply
% equation of resistance in linear region in order to define aspect ratio of M8
s8 = inv( k8 * rz * (vgs10 - vt10) );
fprintf('\nfor transistor M8, aspect ratio, S8=%3.4f Adim. \n', s8);

%*************** option for changing aspect ratio S8
opc = input('do you want to modify aspect ratio of M8 (y/n) ?? ','y');
if (opc=='y') | (opc=='Y')
    fprintf('input new value of S8 (S8=W8/L8, non-dimensional) \n');
    s8 = input('>>> ');
    fprintf('new aspect ratio of M8 S8=%3.4f Adim.', s8);
end;

%*************** define aspect ratio of M11
s11 = ( i11 * s6 ) / i6;
fprintf('\nfor transistor M11: drain current, id11=%3.4e Amperes
\naspect ratio, S11=%3.4f Adim. \n', i11, s11);

%*************** option for changing aspect ratio S11
opc = input('do you want to change aspect ratio of M11 (y/n) ?? ','y');
if (opc=='y') | (opc=='Y')
    fprintf('input new value of S11 (S11=W11/L11, non-dimensional) \n');
    s11 = input('>>> ');
    fprintf('new aspect ratio of M11 S11=%3.4f Adim.', s11);
end;

%*************** define aspect ratio of M9 and S12
s12 = s5;
s9 = ( i10 * s5 ) / i5;
fprintf('\nfor transistor M9: current drain, id9=%3.4e Amperes
\naspect ratio, S9=%3.4f Adim. \n', i9, s9);

%*************** option for changing calculated value of aspect ratio of S9
```

```
opc = input('do you want to change aspect ratio of M9 (y/n) ?? ','y');
if (opc=='y') | (opc=='Y')
    fprintf('input new value of S9 (S9=W9/L9, non-dimensional) \n');
    s9 = input('>>> ');
    fprintf('new aspect ratio of M9, S9=%3.4f Adim.', s9);
end;

%*************** comparing RHPzero from compensation resistance and pole, p2
rz_compara = inv( k8 * s8 * (vgs10 - vt10) );
z1_compara = -inv( ( rz*cc ) - ( cc/gm6 ) );
delta_p = abs( z1_compara - p2 );
fprintf('\ncomparing pole2 and zero1 for compensation with compensation resistance,
\nRz=%3.4e Ohm
\ncalculated value for zero is z1=%3.4e Rad/Seg
\ncalculated value for pole2 is, p2 = %3.4e Rad/Seg', rz, z1_compara, p2);
fprintf('\nthe difference between pole, p2, and compensation zero, z1, is
\nDeltaP=%3.4e Rad/Seg', delta_p);

%*************** calculating transistors width
w_8 = s8 * l_8;         %***** width of M8 [meters]
w_9 = s9 * l_9;         %***** width of M9 [meters]
w_10 = s10 * l_10;         %***** width of M10 [meters]
w_11 = s11 * l_11;         %***** width of M11 [meters]
w_12 = s12 * l_12;         %***** width of M12 [meters]

fprintf('\n \naspect ratio of transistors. given an established  length, the width of
\nevery component is obtained');
fprintf('\ntransistor    aspect ratio    witdh       lenght');
fprintf('\n    M8           %3.4f          %3.4e       %3.4e',s8, w_8, l_8);
fprintf('\n    M9           %3.4f          %3.4e       %3.4e',s9, w_9, l_9);
fprintf('\n    M10         %3.4f          %3.4e       %3.4e',s10, w_10, l_10);
fprintf('\n    M11         %3.4f          %3.4e       %3.4e',s11, w_11, l_11);
fprintf('\n    M12         %3.4f          %3.4e       %3.4e',s12, w_12, l_12);

printf('\n \n');

% s8 w8 l8 s9 w9 l9 s10 w10 l10 s11 w11
% l11 s12 w12 l12 Vg8 Rz p2 z1 delta_p
fprintf('%3.4f %3.4f %2.2f %3.4f %3.4f %2.2f %3.4f %3.4f %2.2f %3.4f %3.4f
\n%2.2f %4.4f %5.5f %2.2f %3.4f %3.4f %3.4f %3.4f',s8,w_8*(10^6),l_8*(10^6),
s9,w_9*(10^6),l_9*(10^6),s10,w_10*(10^6),l_10*(10^6),s11,w_11*(10^6),
```

```
l_11*(10^6),s12,w_12*(10^6),l_12*(10^6),rz_compara*(10^-3),p2*(10^-6),
z1_compara*(10^-6),delta_p*(10^9));
fprintf('\n \nend of program.. \n');
```

B.3 Octave Script for Bias Current Stage Design

```
% curr1.m, obtained from final_current_source.m
% created by Luis Saracho, on oct-16-2007
% last updated on march-20-2008
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
% this program defines aspect ratios for transistors M8, M9, M10, M11 from the new
% block used for RHPzero compensation resistance biasing circuit. the obtained block
% is applied to the two-stage CMOS OTA design.
% working file

%*************** process parameters
%kp = 50; % [uA/volts^2] p-type transconductance parameter
kn = 110; % [uA/volts^2] n-type transconductance parameter
vtn = 0.7;   % [volts] n-type transistor threshold voltage
%vtn_max = vtn + 0.15;   % maximum n-type threshold voltage
%vtn_min = vtn - 0.15;   % minimum n-type threshold voltage
%vtp = -0.7;   % [volts] p-type transistor threshold voltage
%vtp_max = vtp - 0.15;   % maximum p-type threshold voltage
%vtp_min = vtp + 0.15; % maximum p-type threshold voltage

%*************** variables
iq_base = 15; % [uAmp] source current
l_baseq = 0.5; % [uMetros] transistors length
w_baseq = 50;       % [uMetros] transistors width
rq = 50000; % [Ohm] magnitude of resistance connected to the circuit
v_r = 0.186; % [Volts] transistors linearization voltage (from bias voltage source)

%*************** parameters assignaion and change of units
iq = iq_base * (1e-6);  % definition of source current and conversion to [Amp]
k1q = kn * (1e-6);      % definition of k1 and conversion to [amp/volts^2]
l_1q = l_baseq * (1e-6);% definition of Mq1 length and conversion to [Metros]
w_1q = w_baseq * (1e-6);% definition of Mq1 width and conversion to [Metros]
vt1q = vtn; % definition of threshold voltage [Volts]

k_rq = kn * (1e-6); % aspect ratio of transistor/resistance
vgs_rq = v_r; % gate votlage of transistor/resistance
vt_rq = vtn; % threshold voltage of transistor/resistance

opc = 's';
while (opc == 's') || (opc =='S')
```

```
%*************** definition of BETA
   beta_q = k1q * w_1q / l_1q;

%*************** obtaining current magnitud from BETA and R
   i_calc = (vt1q/rq) + inv( beta_q * rq* rq ) +
( inv(rq) * sqrt(((2*vt1q) / ( beta_q * rq )) + inv( beta_q * beta_q * rq * rq )));
   fprintf('\n \nlength of transistors, L=%3.3f uMeters,
\nW=%3.3f uMeters', l_1q/(1e-6) , w_1q/(1e-6) );
   fprintf('\naccording to parameters
\nBeta=%3.4e Amp/Volts^2 \nResistance=%3.4e Ohm
\nthe calculated current is Iq=%3.4e Amp', beta_q, rq, i_calc);
   fprintf('\nrequired current is I=%3.4e Amp', iq);
   delta_iq = abs( iq - i_calc );
   fprintf('\ndifference between required current and calculated current,
\nDeltaI=%3.4e Amp \n', delta_iq);

%*************** option of changing the value of BETA and R
       opc = input('do you want to change BETA and/or resistance R (y/n)?? ','y');
       if (opc=='y') | (opc=='Y')
           fprintf('input new value for L1_q (uMeters) \n');
           l_1q = input('>>> ');
           l_1q = l_1q * (1e-6);

           fprintf('input new value for W1_q (uMeters) \n');
           w_1q = input('>>> ');
           w_1q = w_1q * (1e-6);

           fprintf('input new value for R (Kohm) \n');
           rq = input('>>> ');
           rq = rq * (1e3);

           fprintf('new defined values, \nW1_q=%3.4f uMeters \nL1_q=%3.4f uMeters
\nR=%3.4f Kohm', (w_1q/(1e-6)), (l_1q/(1e-6)), (rq/(1e3)));
       end;
end;

%*************** define characteristics of transistor that will substitute resistance
% code lines from final_null_resistor.m
% data required for obtaining Vgs_Rq
i6 =  27.5e-6;
```

```
i10 = 5e-6;
i11 = i10;
k10 = 110e-6;
k11 = 110e-6;
s6 = 94;
s10 = 1;
vt10 = 0.7;
vt11 = 0.7;
vgs10 = sqrt( ( 2 * i10 ) / ( k10 * s10 ) ) + vt10
s11 = ( i11 * s6 ) / i6
vgs11 = sqrt( ( 2 * i11 ) / ( k11 * s11 ) ) + vt11
vgs_rq = vgs10 + vgs11

%*************** define S_rq
fprintf('\ndefinition of size for the transistor that will substitute resistance Rq');
s_rq = inv( k_rq * rq * ( vgs_rq - vt_rq ) );
fprintf('\nrtransistor aspect ratio, M_Rq, \nS_rq=%3.4f Adim. \n', s_rq);

%*************** option of changing the value of the aspect ratio, S_Rq calculated
opc = input('do you want to change aspect ratio S_Rq (y/n)?? ','y');
if (opc=='y') | (opc=='Y')
    fprintf('input new value for S_Rq (S_Rq=W_Rq/L_Rq non-dimensional) \n');
    s_rq = input('>>> ');
    fprintf('new aspect ratio for M7, S7= %3.4f Adim.', s_rq);
end;

fprintf('\ndefine minimum length, L_Rq (uMeters) \n');
l_rq = input('>>> ');
l_rq = l_rq * (1e-6);
w_rq = s_rq * l_rq;

fprintf('\naspect ratio of transistor, M_Rq, \nS_Rq=%3.4f Adim.
\nwidth, W_Rq=%3.4f um
\nlength, L_Rq=%3.4f um', s_rq/(1e-6), w_rq/(1e-6), l_rq/(1e-6));

fprintf('\nend of program.. \n');
input('press enter..');
```

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